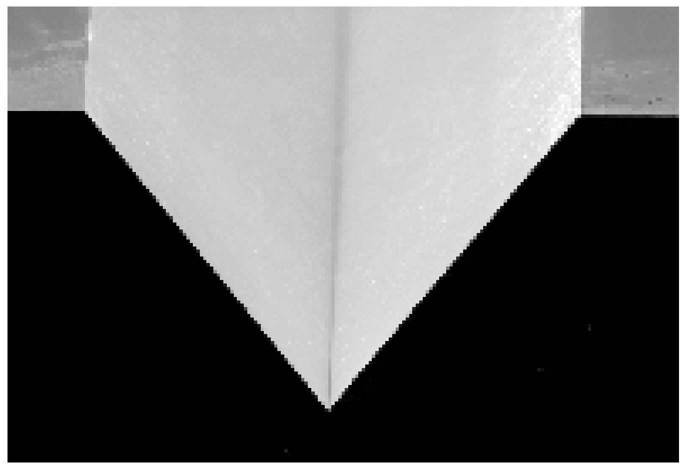

Bulk Silicon Micromachining

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Micro Actuators, Sensors, Systems Group
University of Illinois at Urbana-Champaign

Outline

- Types of bulk micromachining
  - silicon anisotropic etching
    - crystal orientation
  - isotropic etching of liquid and gas phase etchants
- Silicon anisotropic etching
  - influence on etch rate by orientation
  - influence on etch rate by doping concentration
- Etching simulation with ACES

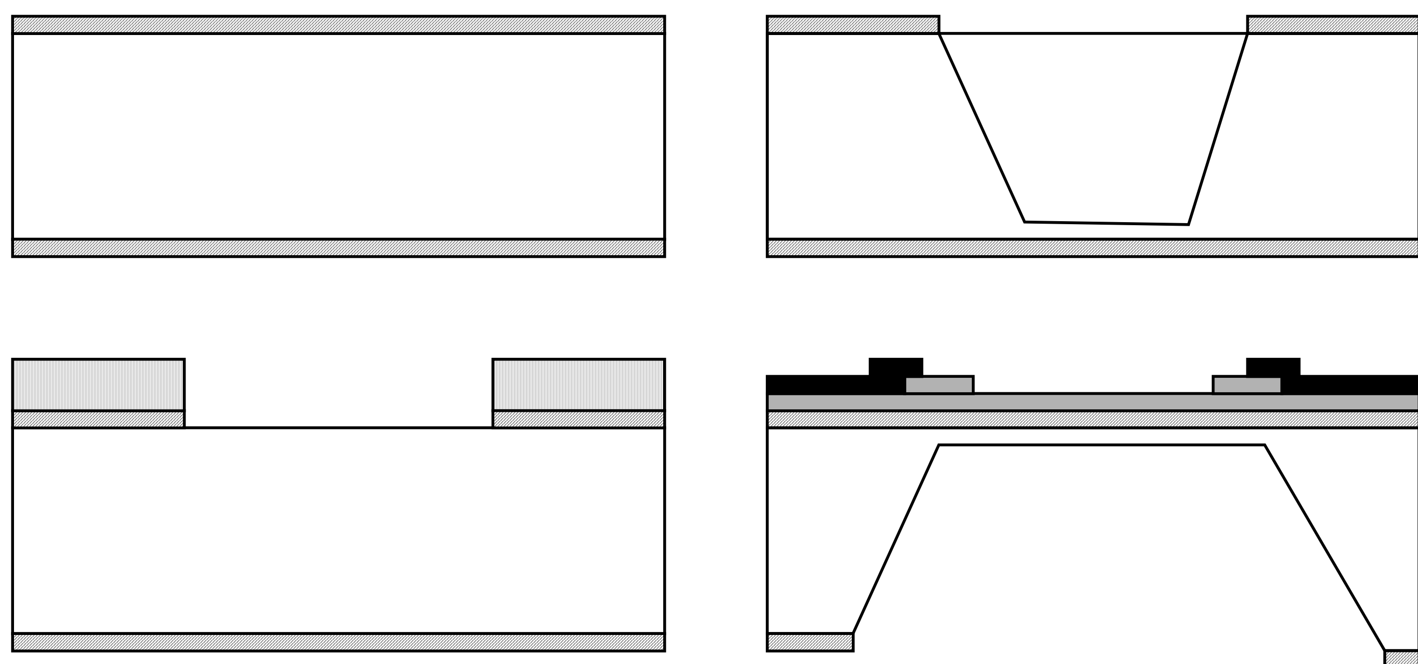
Definition

- Silicon bulk micromachining
  - processes that involve partial removal of bulk material in order to create three dimensional structures or free devices.

- General micromachining
  - machining process that involves removal of substrate materials in order to render functional devices.

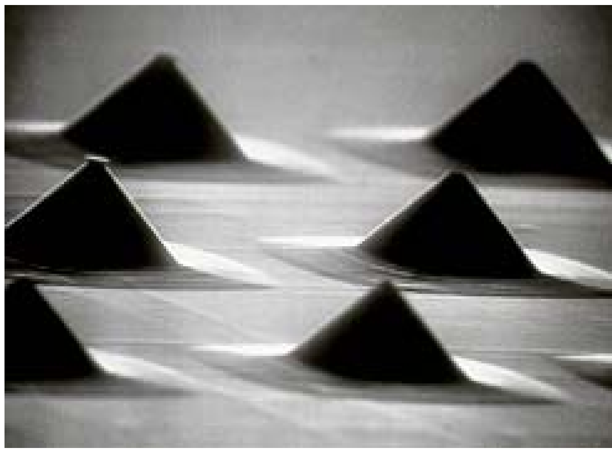
Example of a Bulk Etching

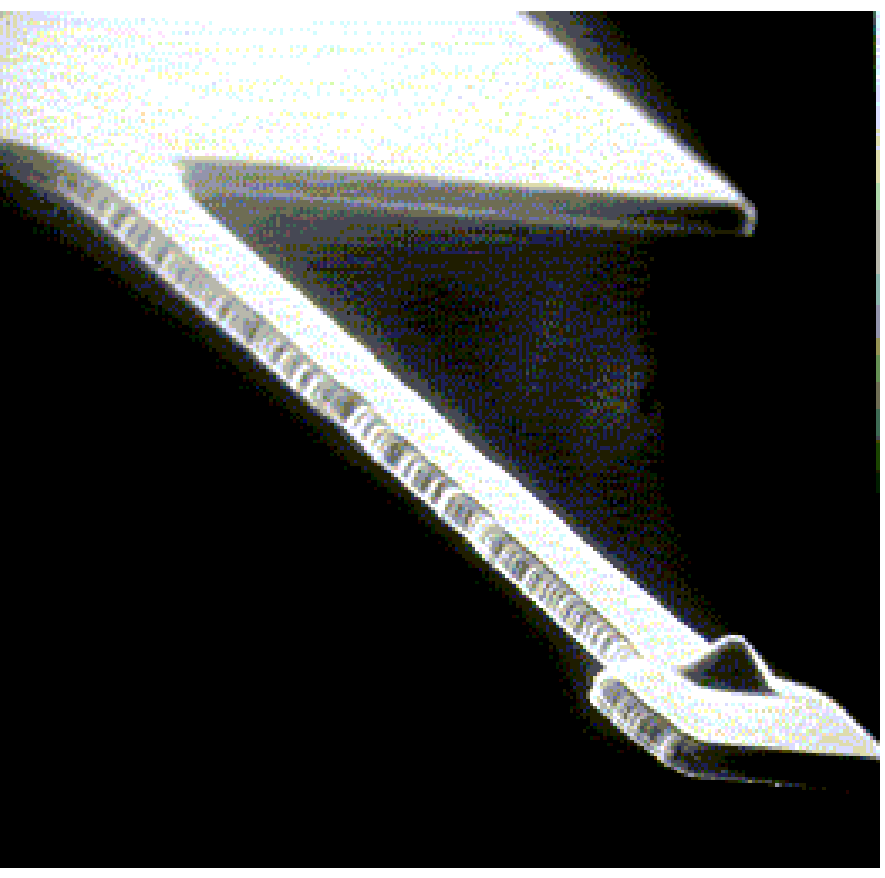
- Schematic diagram of the process for a pressure sensor.



Example of Bulk Etching

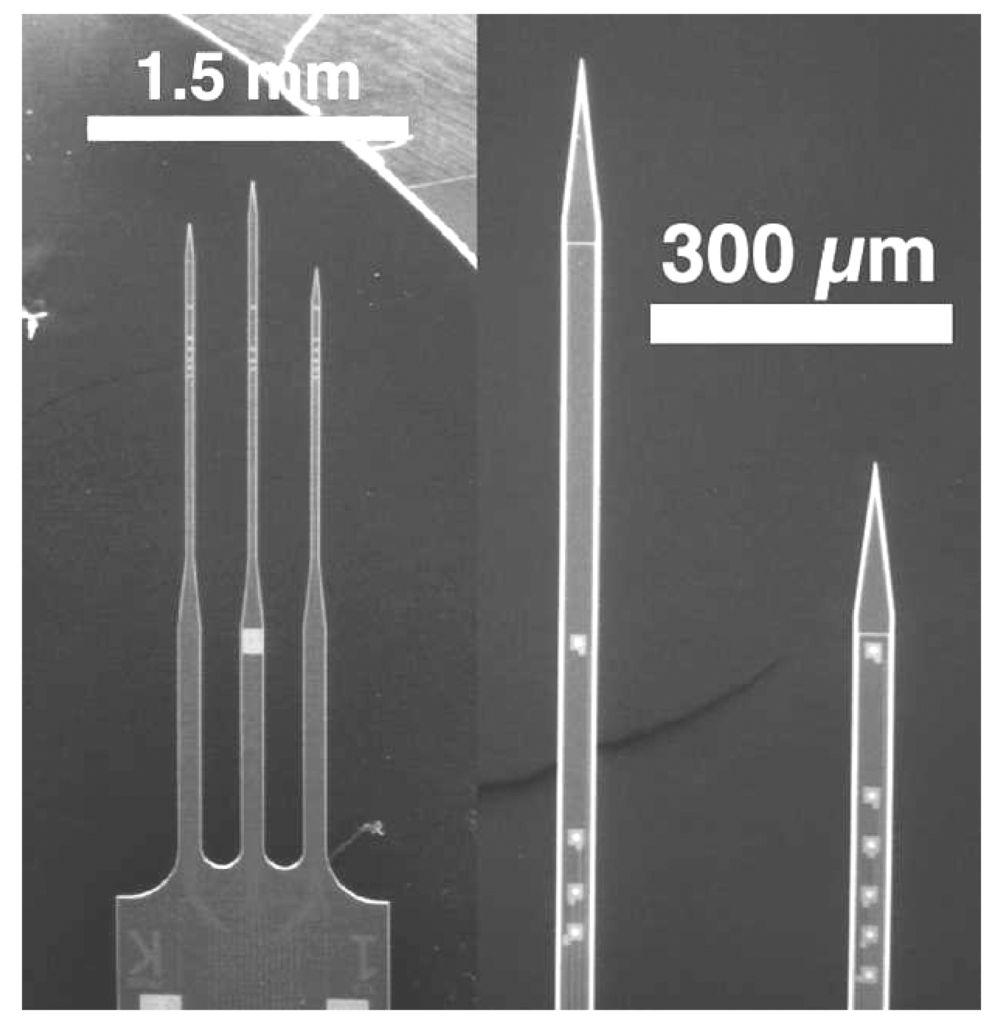
- Micromachined AFM/STM probe





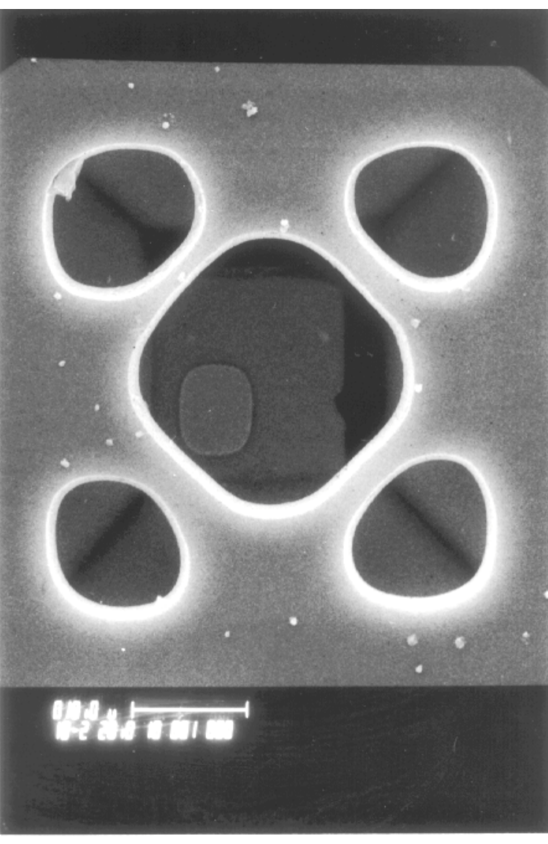
Example of Bulk Machining

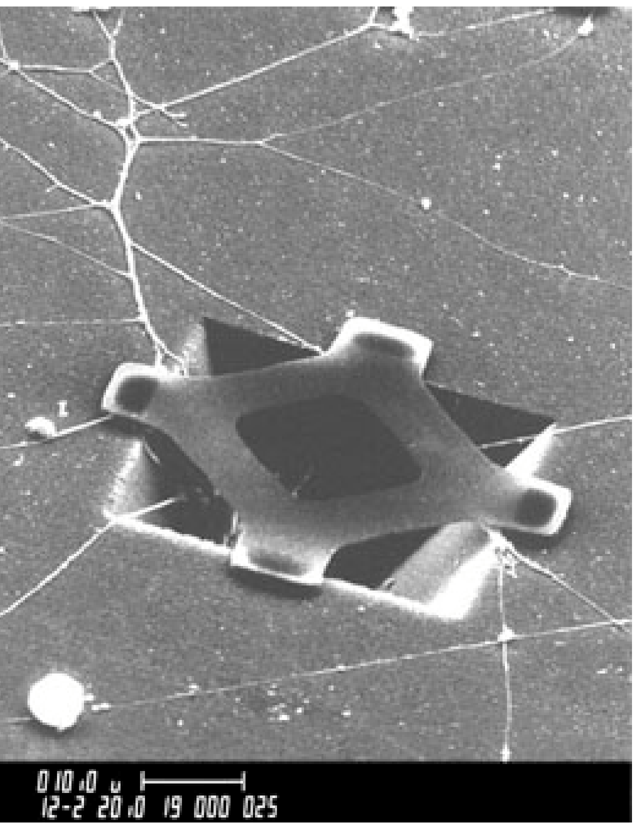
- Stanford University Neuron Probe
  - Development of complete analog signal processing electronics package.
  - Demonstration of successful, repeated recordings from rat cerebellar cortex and tissues slices with multi-channel data acquisition.
  - A combination of plasma etching and selective wet etch stopping is used to define the overall shape of the probes.
  - Multi-level metallization with thin-film iridium microelectrode sites allows for small and constant probe cross section.

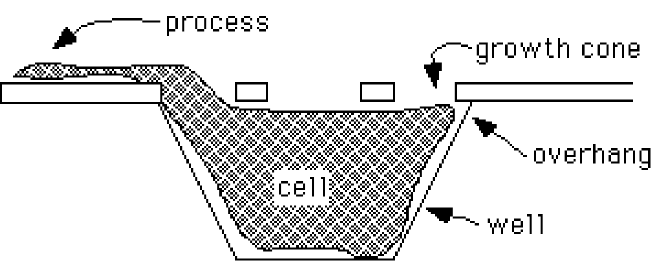


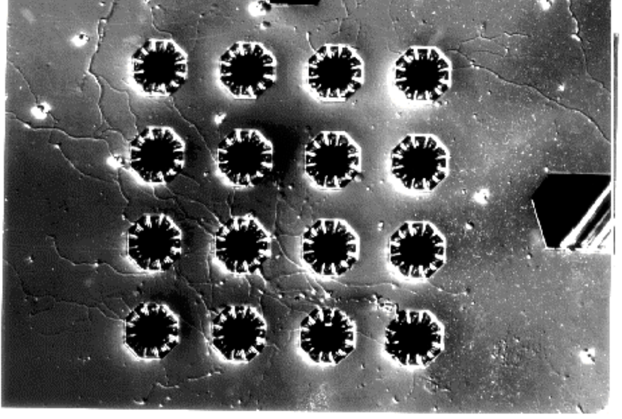
Micromachined Neuron Wells

- In order to really get at the dynamics of a functioning neuronal network, you need to know what all the different components are doing at the same time. To study plasticity, where interconnections between the neurons change based on the activity patterns, you need to be able to influence the cells without damaging them. To study development, where the various pieces of the network are changing, you also need to be able to measure the activities of the same neurons over time. Otherwise you're stuck making statistical analyses of the activities, which is far less helpful.



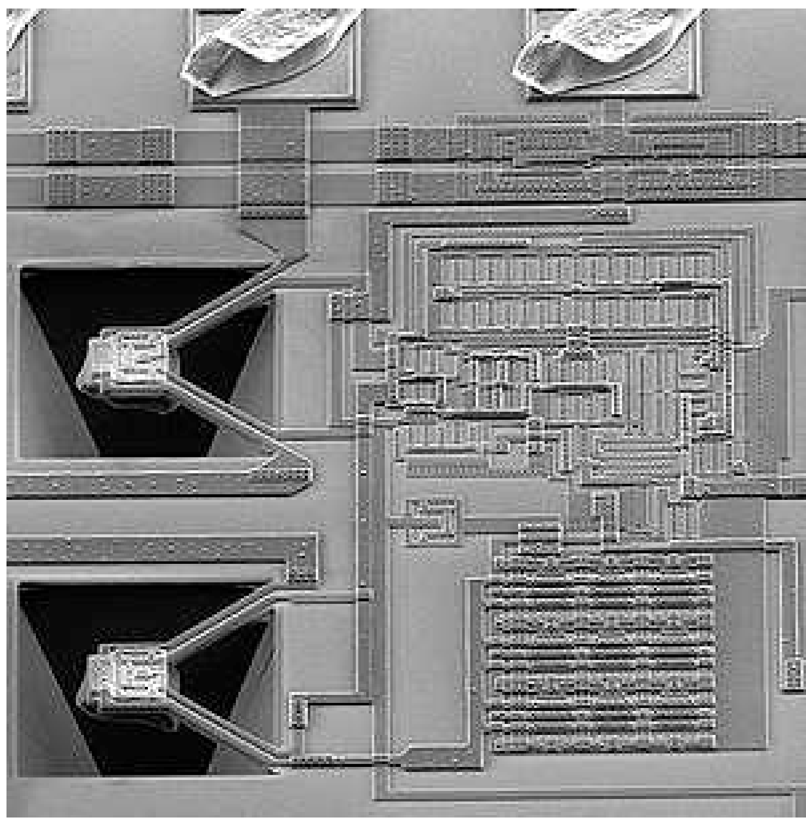


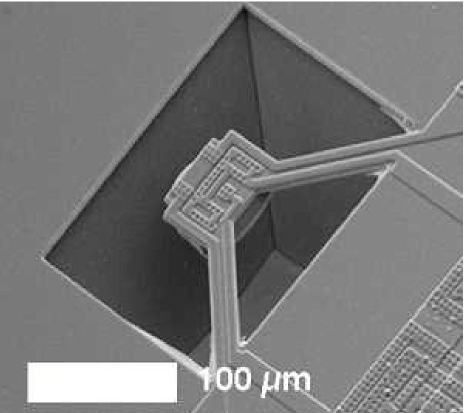




Stanford Thermal RMS Converter

- Using a standard CMOS process, n-wells are biased so that they self-passivate while selectively exposed p-silicon (substrate) is etched, resulting in single-crystal silicon islands that are suspended above etched pits by oxide/aluminum members.
- This approach allows for thermal isolation of entire active circuits or any subset of them, based on components that can be fabricated in an n-well.
- Demonstration of very highly thermally isolated (60,000 degrees/Watt) single-crystal silicon islands.
  - Demonstration of thermally-stabilized band-gap voltage reference. Demonstration of >400 MHz, 60 dB dynamic range thermal RMS converter with on-chip CMOS servo circuits.
  - Demonstration of digitally controlled, fully integrated thermal (Pirani-type) vacuum sensor.

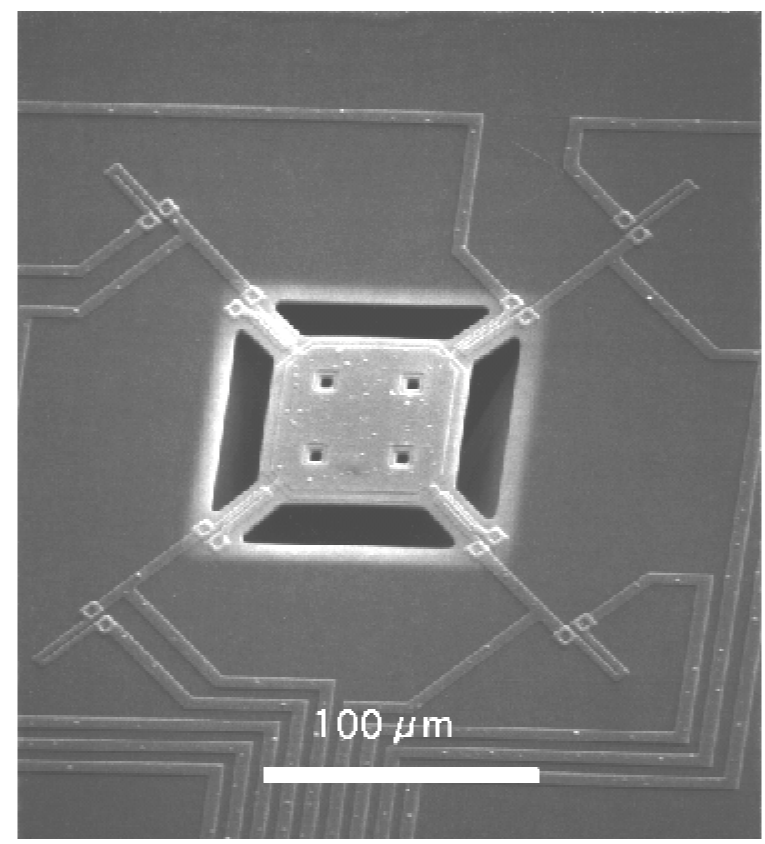




http://transducers.stanford.edu/stl/Projects/electro-Erno_K.html

Example of Bulk Micromachining
Micro tactile sensor

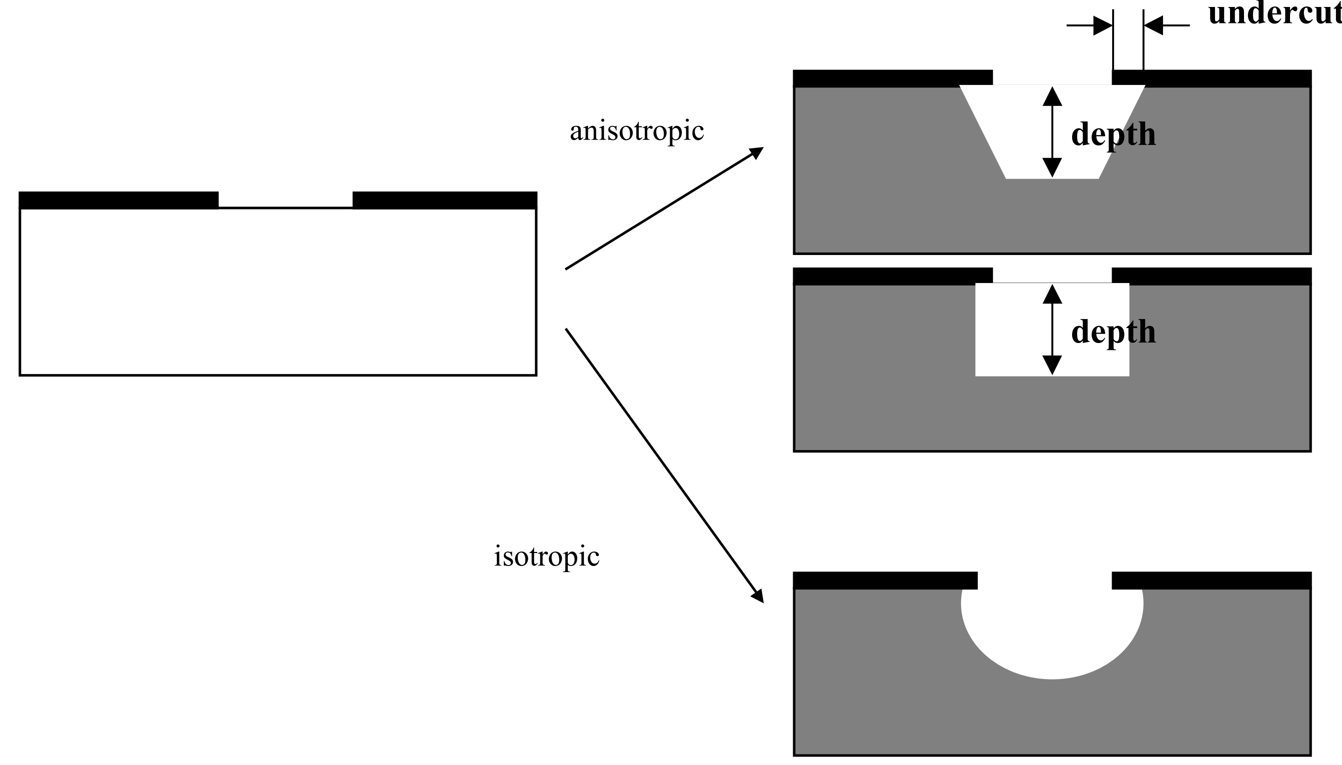
- Goals
  - Development of a CMOS-compatible tactile sensor with independent x- and y-axis shear and normal force sensing capability.
  - Integration of all necessary multiplexing and power switching circuitry onto a single chip to enable a large (approximately 2 X 2 cm) active tactile sensor array.



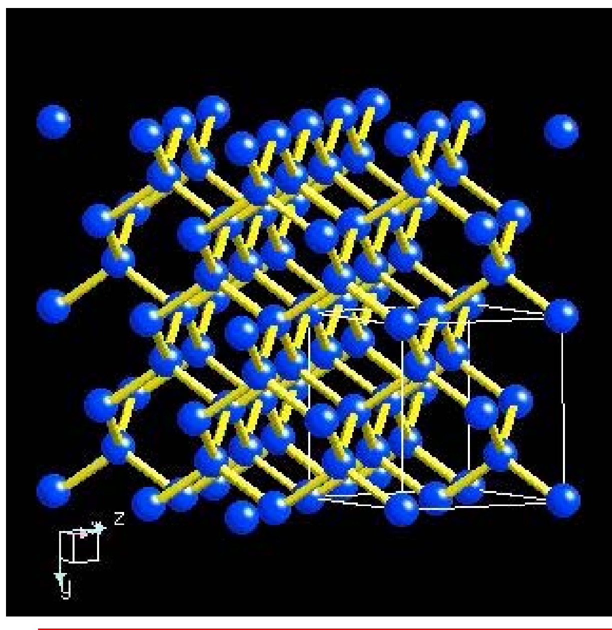
- **Technical Approach:**
  - Composite (silicon dioxide/polysilicon/silicon dioxide/aluminum/silicon nitride sandwitch) plates suspended by four bridges with embedded strain sensing polysilicon piezoresistors. Shuttle plate is allowed to translate by an undercut etch of the underlying bulk silicon by with a wet a tetramethyl ammonium hydroxide (TMAH) etch.
  - By algebraically combining the output signals from the four strain gauges, independent measures of x- and y-axis shear and normal forces is available.
  - The fabrication process used is fully CMOS compatible.

Anisotropic Etching

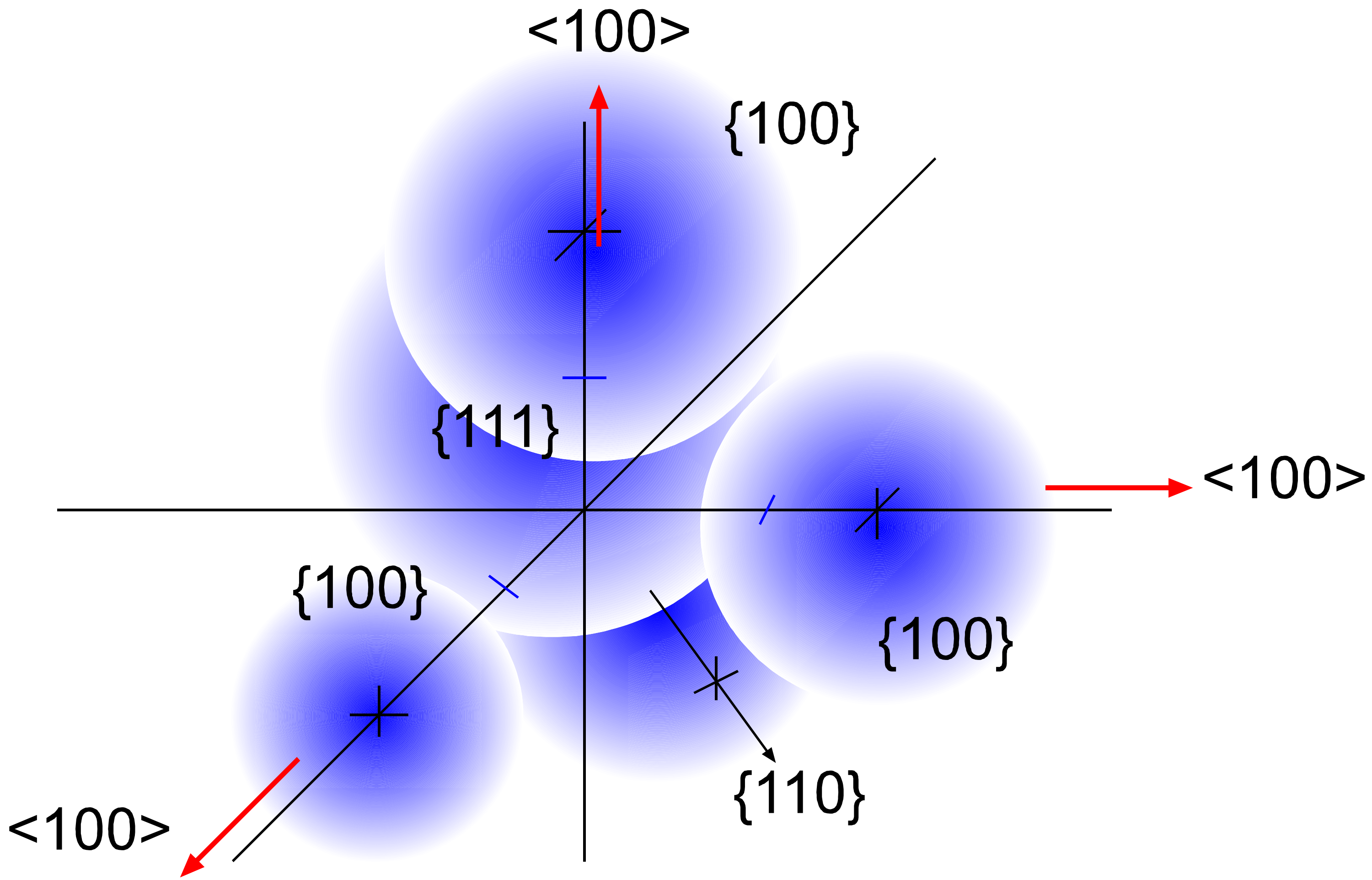
- Etching rate is dependant on the crystal orientation.
- The difference in etch rate is used creatively to generate unique 3D structures.



Silicon <110> View

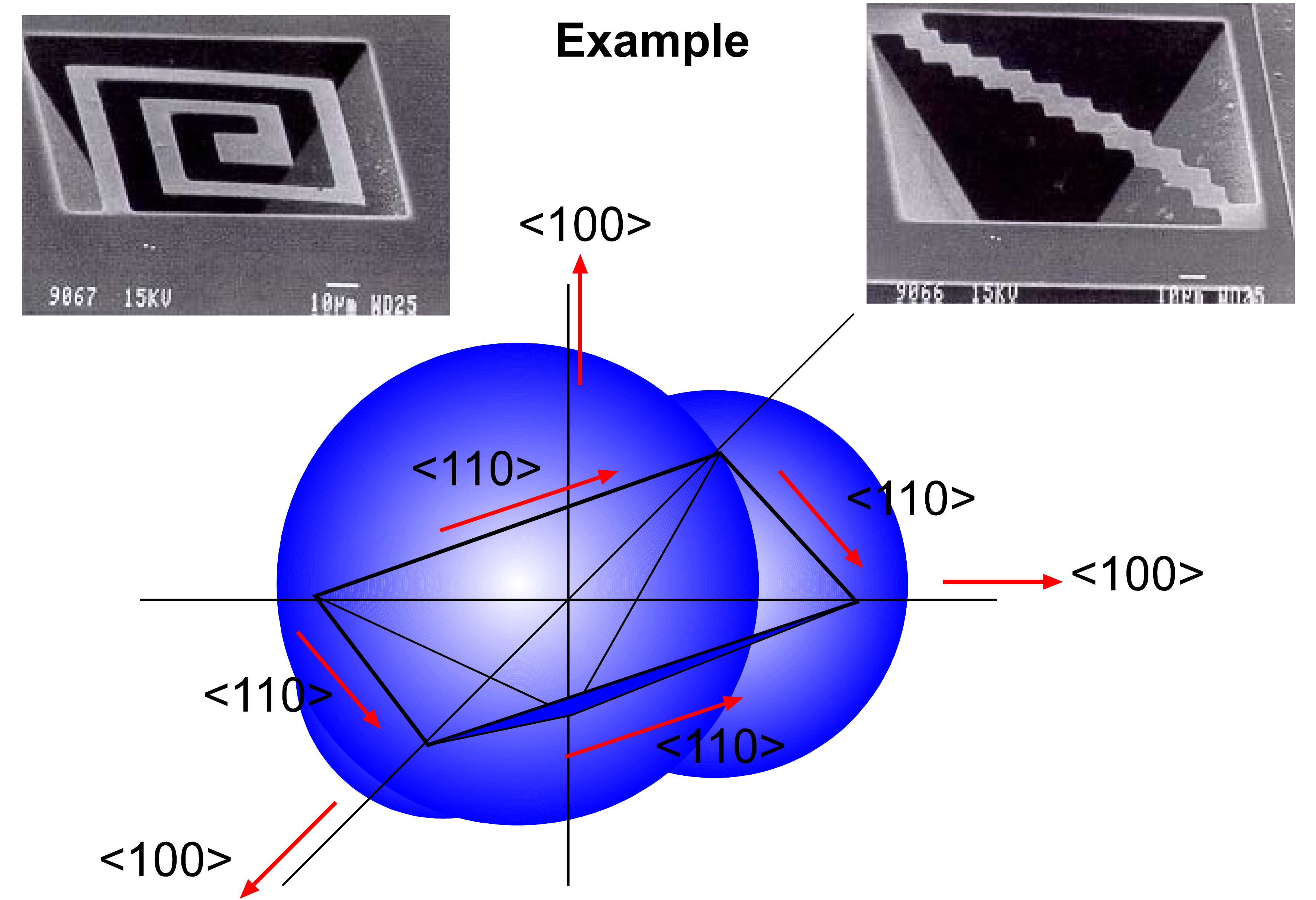


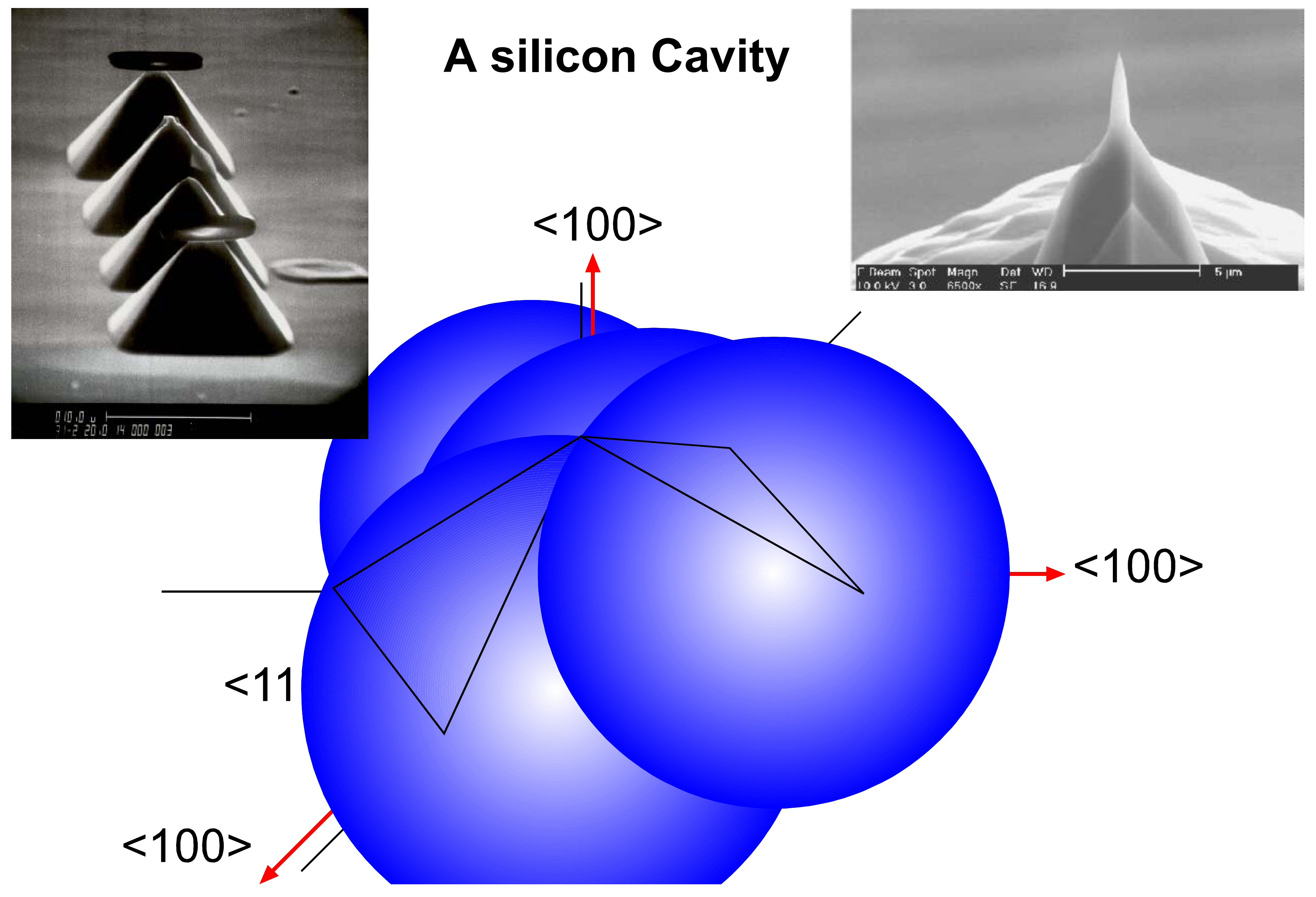
Silicon Wafer Orientation



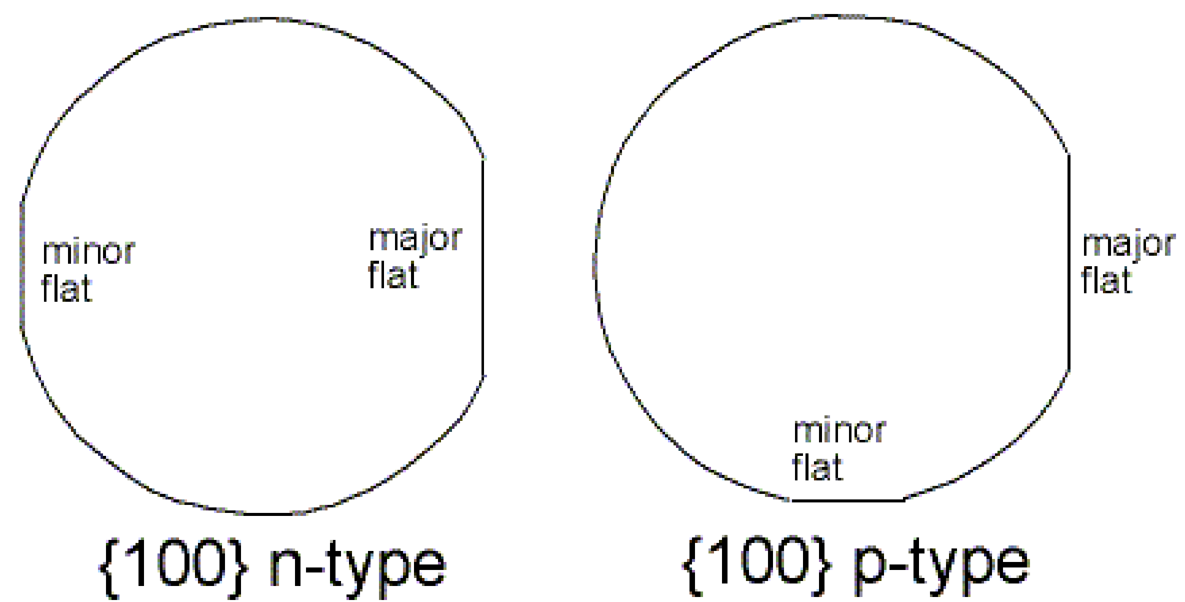
Lattice Forest

Wafer Orientation	[100] {100}	[110] {100}	[100] {110}	[110] {111}
3D Lattice and top surface	x y z	x y z	z x y	y z x
Lattice top view	z x y	z x y	z x y	z x y


Example
9867 15KV
10µm WD25
9866 15KV
<100>
<110>
<110>
<100>
<110>
<110>
<100>

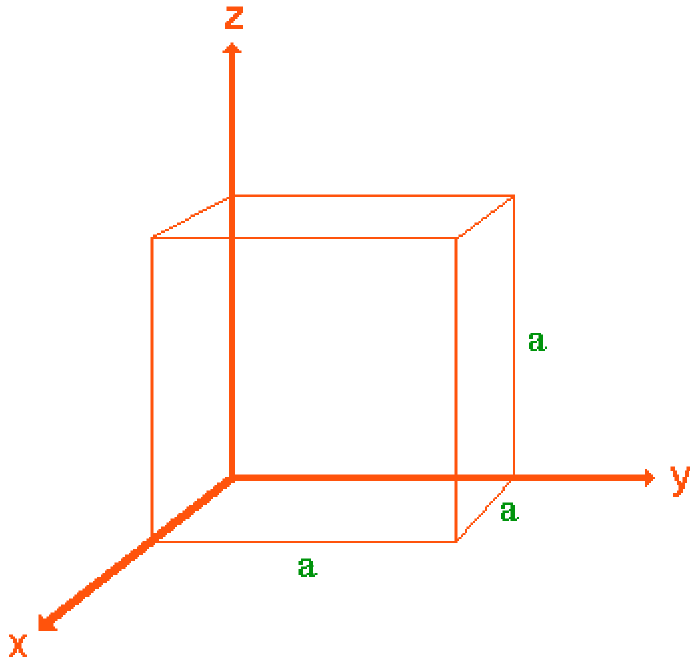

A silicon Cavity
<100>
<100>
<11
<100>
5 µm

Telling Wafer Orientation by Flats



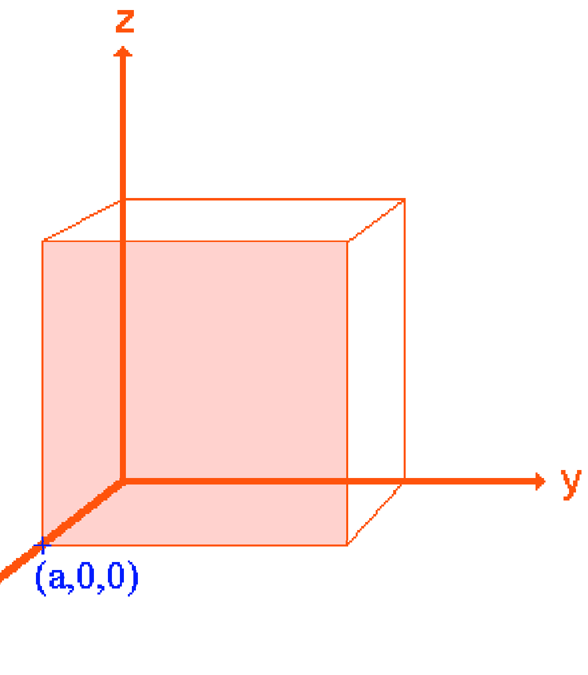
Crystal Orientation - Miller Index

- The orientation of a surface or a crystal plane may be defined by considering how the plane (or indeed any parallel plane) intersects the main crystallographic axes of the solid. The application of a set of rules leads to the assignment of the Miller Indices , (*hkl*) ; a set of numbers which quantify the intercepts and thus may be used to uniquely identify the plane or surface.
- The following treatment of the procedure used to assign the Miller Indices is a simplified one (it may be best if you simply regard it as a "recipe") and only a **cubic** crystal system (one having a cubic unit cell with dimensions *a* x *a* x *a*) will be considered.



Construction of Miller Index

- The procedure is most easily illustrated using an example so we will first consider the following surface/plane:
- **Step 1** : *Identify the intercepts on the x- , y- and z- axes.*
  - In this case the intercept on the x-axis is at x = a (at the point (a,0,0)), but the surface is parallel to the y- and z-axes - strictly therefore there is no intercept on these two axes but we shall consider the intercept to be at infinity (∞) for the special case where the plane is parallel to an axis. The intercepts on the x- , y- and z-axes are thus
  - Intercepts : **a** , ∞ , ∞



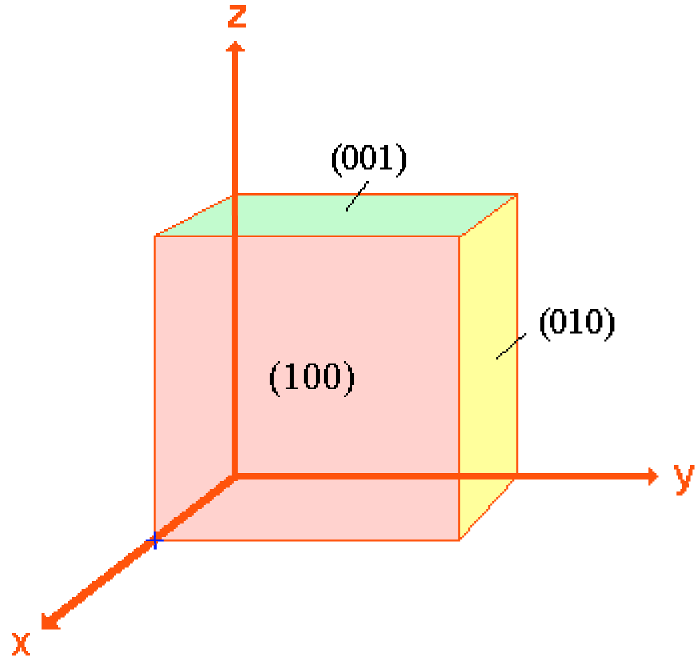
Construction of Miller Index

- **Step 2** : Specify the intercepts in fractional co-ordinates
  - Take the reciprocals of the three integers found in Step 1 and reduce them to the smallest set of integers h, k and l.
  - Fractional Intercepts : **a/a ,** ∞/α, ∞/α ι.ε. 1 , ∞ , ∞
  - Miller Indices : **(100)**
  - So the surface/plane illustrated is the (100) plane of the cubic crystal.

- Check 340 text book for more details; or chapter 2 of binder notes.

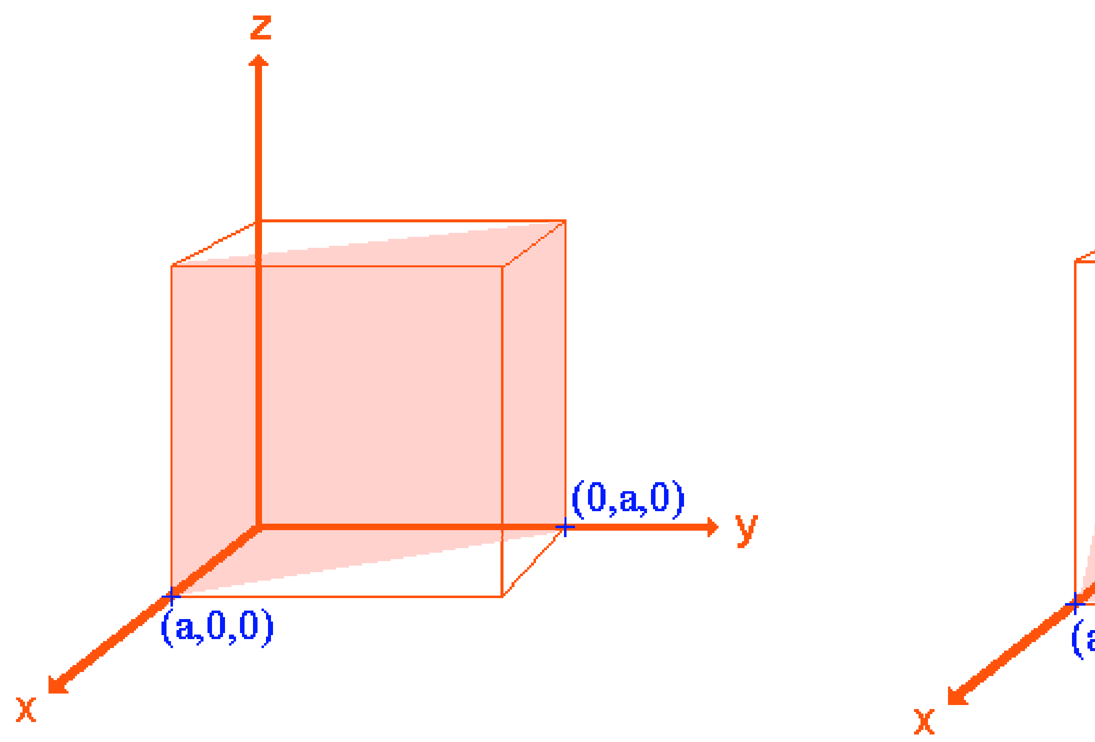
Construction of Miller Index

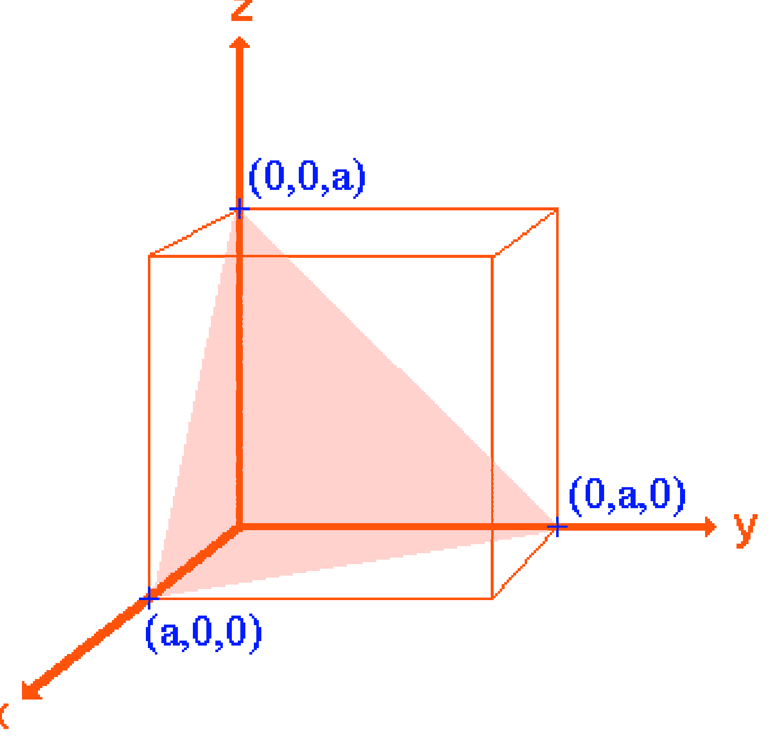
- Equivalent planes
- Three equivalent planes (100), (010) and (001) belong to the {100} family.
  - Notice the notification.



Miller Index

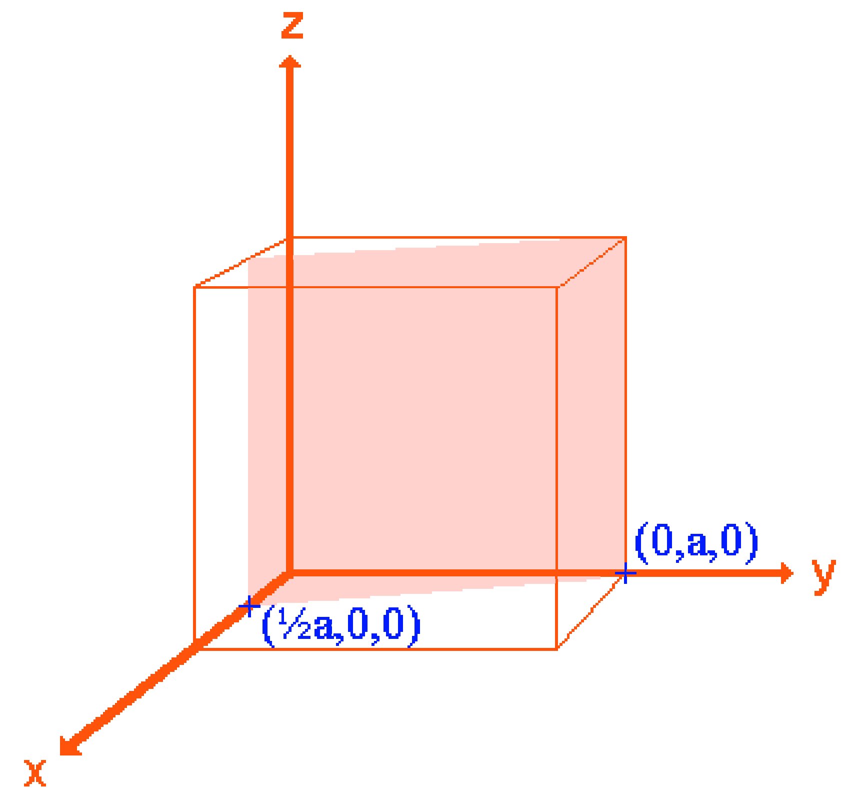
- Other low index planes.





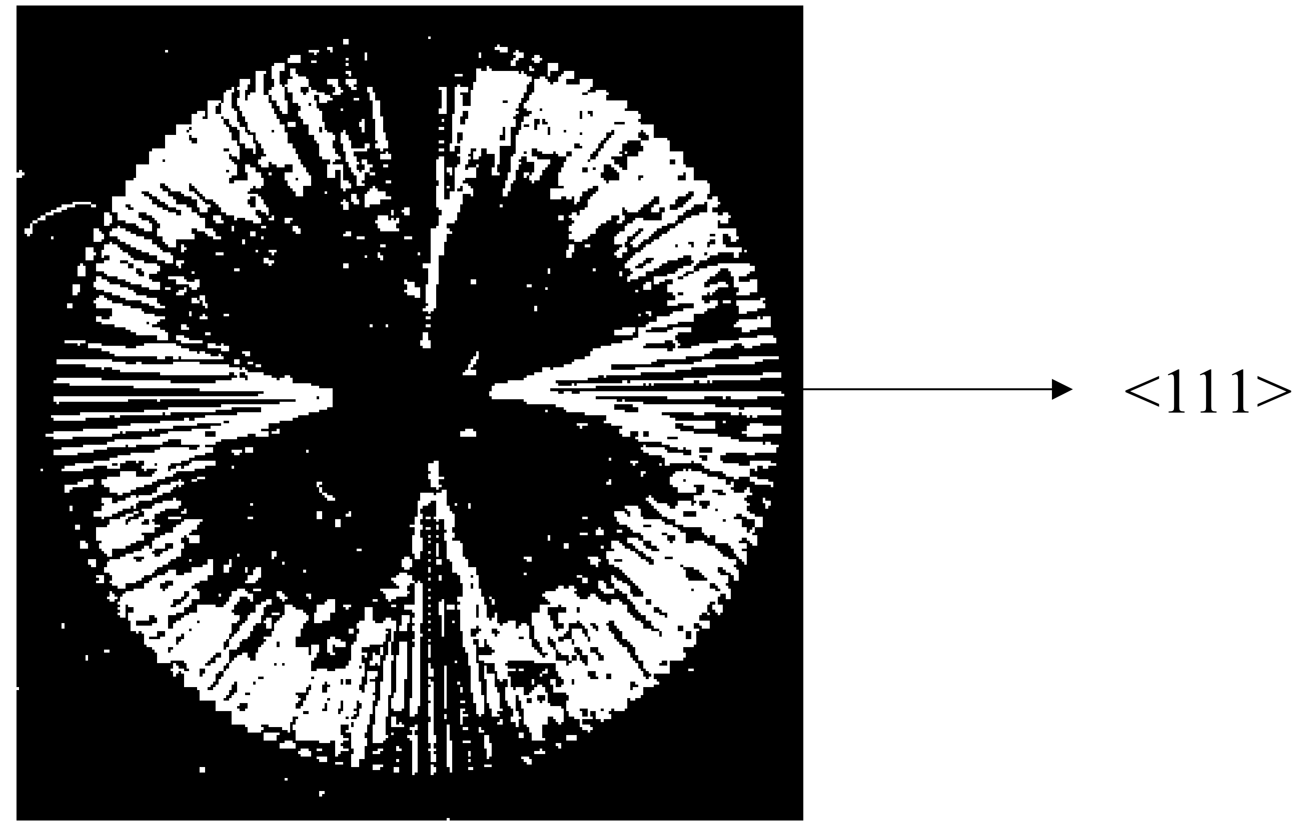
High Index Plane

- Example {211} Plane

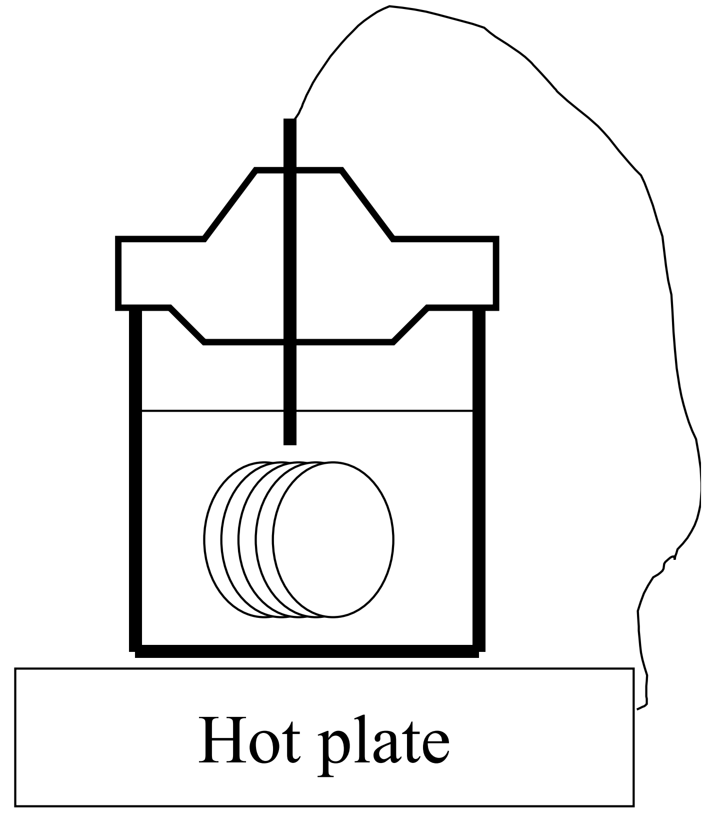


Etch Rate is A Function of Direction

- Etch of wagon-wheel pattern to reveal difference in etch rate is different wafer orientations.



Etching System - Reflux system



Reflux system

Etch in Anisotropic Etchant

- The masked region is not etched.
- The slopped region {111} slows forms but etches slowly.
- The bottom surface {100} etches quickly (tens of micrometers per second).

mask

<110>

<110>

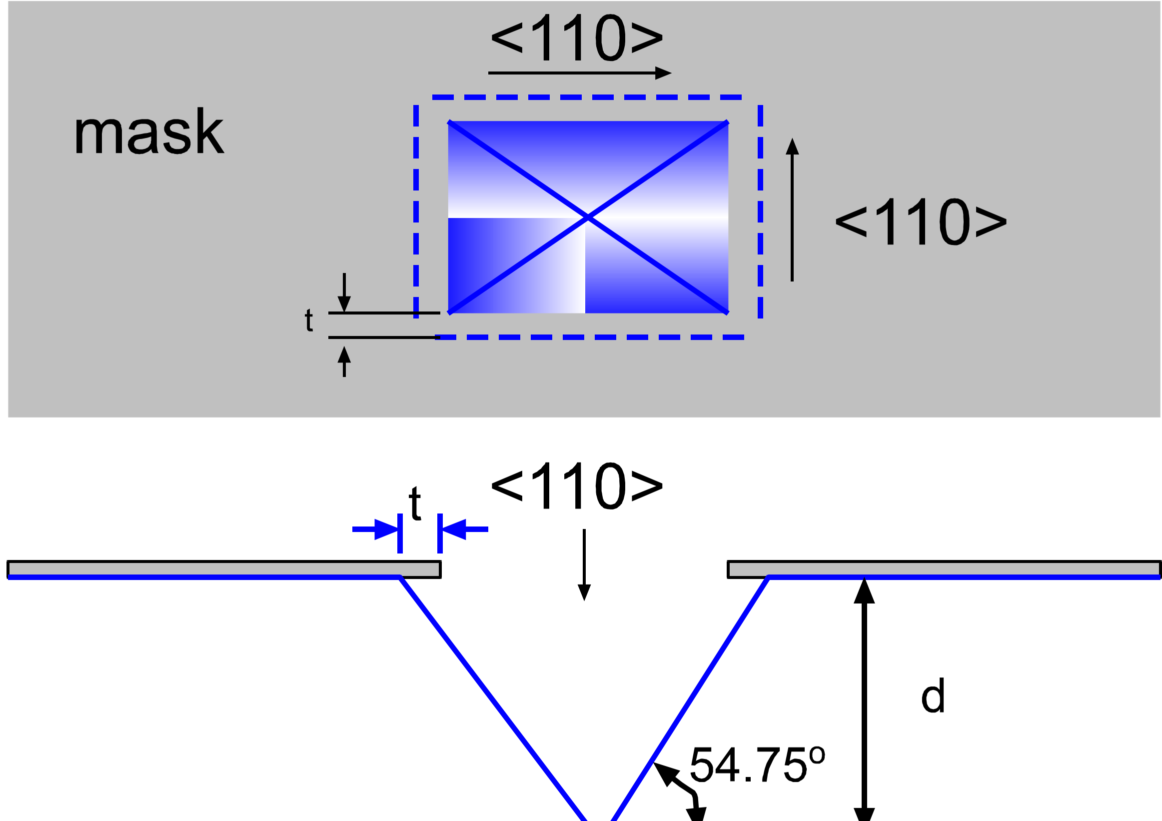
<100>

<111>

<110>

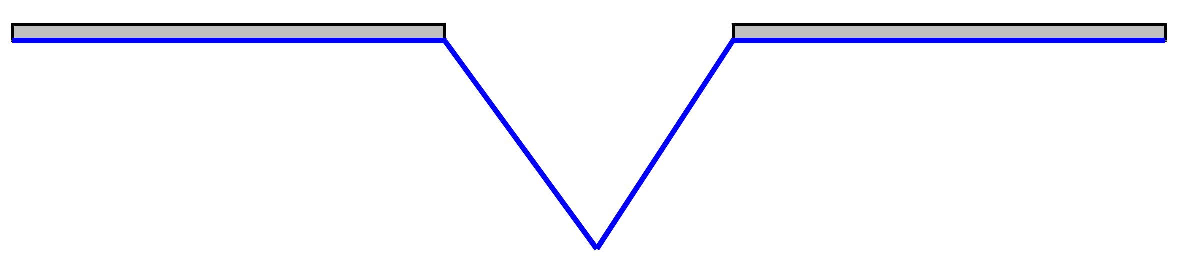
Results after extended etching

- The vertical distance d is etch rate in <100> direction times the duration.
- The lateral distance t is [etch rate in <111> direction times the duration]/sin(54.75).



Idealized Case

- Zero lateral undercut.
- Almost always true as the etch rate ratio of <100> and <111> can reaches several hundred.



Commonly Used Silicon Etchants (Fig. 3, Chapter 8, Binder Handout)

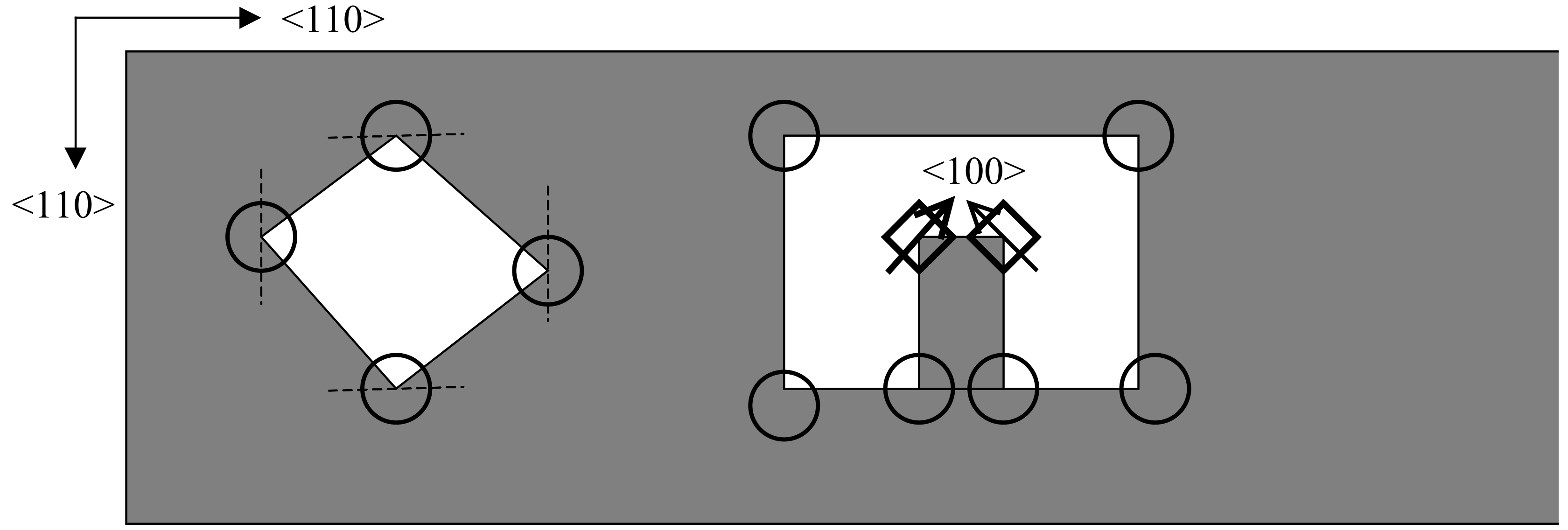
- EDP (Ethylene diamine pyrocatechol) 90° (p. 43)
  - sometimes refers to EPW, Ethylenediamine Pyrocatechol and Water)
  - Etch rate ratio for <100> and <111> is as high as 35:1 or higher (Petersen paper, chpt. 1, Binder notes)
  - Etch rate for silicon nitride and silicon oxide is almost negligible.
    - Even native oxide (see next page) becomes important in processing
  - Highly directional selective, allows cheap oxide as mask.
  - Expensive; chemically unstable.
  - Aging: etch rate and color changes with time after exposure to oxygen.
- KOH (Potassium hydroxide) 75-90° (* p. 36)
  - various concentration can be used, 20-40 wt % is common.
  - Etch rate ratio for ,100> and <111> is also very high (even higher than that of EDP).
  - Etch rate on silicon nitride (LPCVD) is negligible.
  - Etch rate on silicon oxide is not negligible.
    - 14 angstrom/min. (thermally grown oxide quality).
    - e.g. a process last for 10 hours consumes 0.84 μm of oxide.
- Other
  - TMAH (tetramethyl ammonium hydroxide) (* 40)

Commonly Used Isotropic Etchant

- HNA
  - Hydrofluoric acid + Nitric Acid + Acetic acid
  - Various mixing ratios are possible, resulting in different etch rates.
  - Because the solution contains HF, the etch rate on oxide is relatively quick, 300 Angstrom/min.
  - * 32 text book.
- Room temperature process.

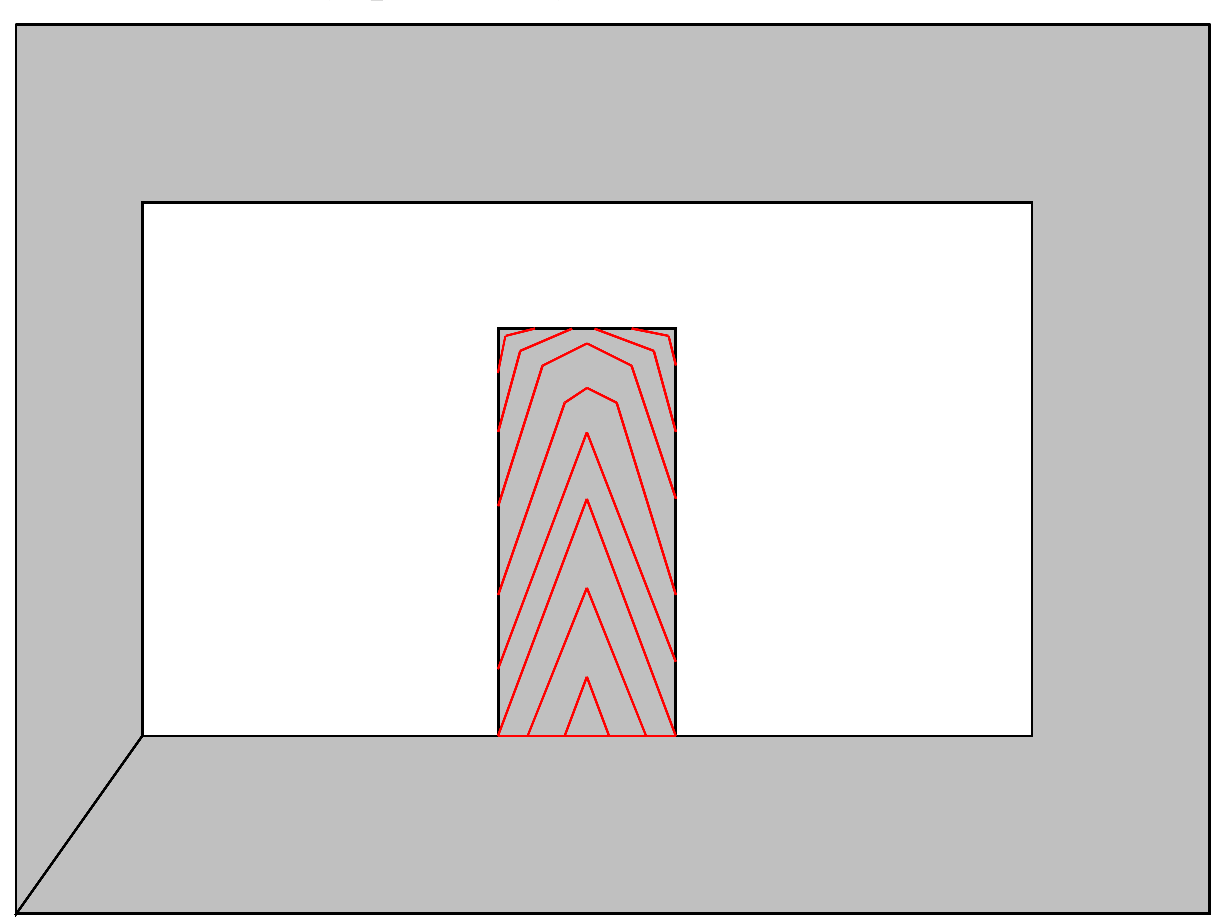
Etching Rules

- For convex corners, the fastest etching planes dominate the three-dimensional shape.
- For concave corners, the slowest etching planes dominate the three dimensional shape.

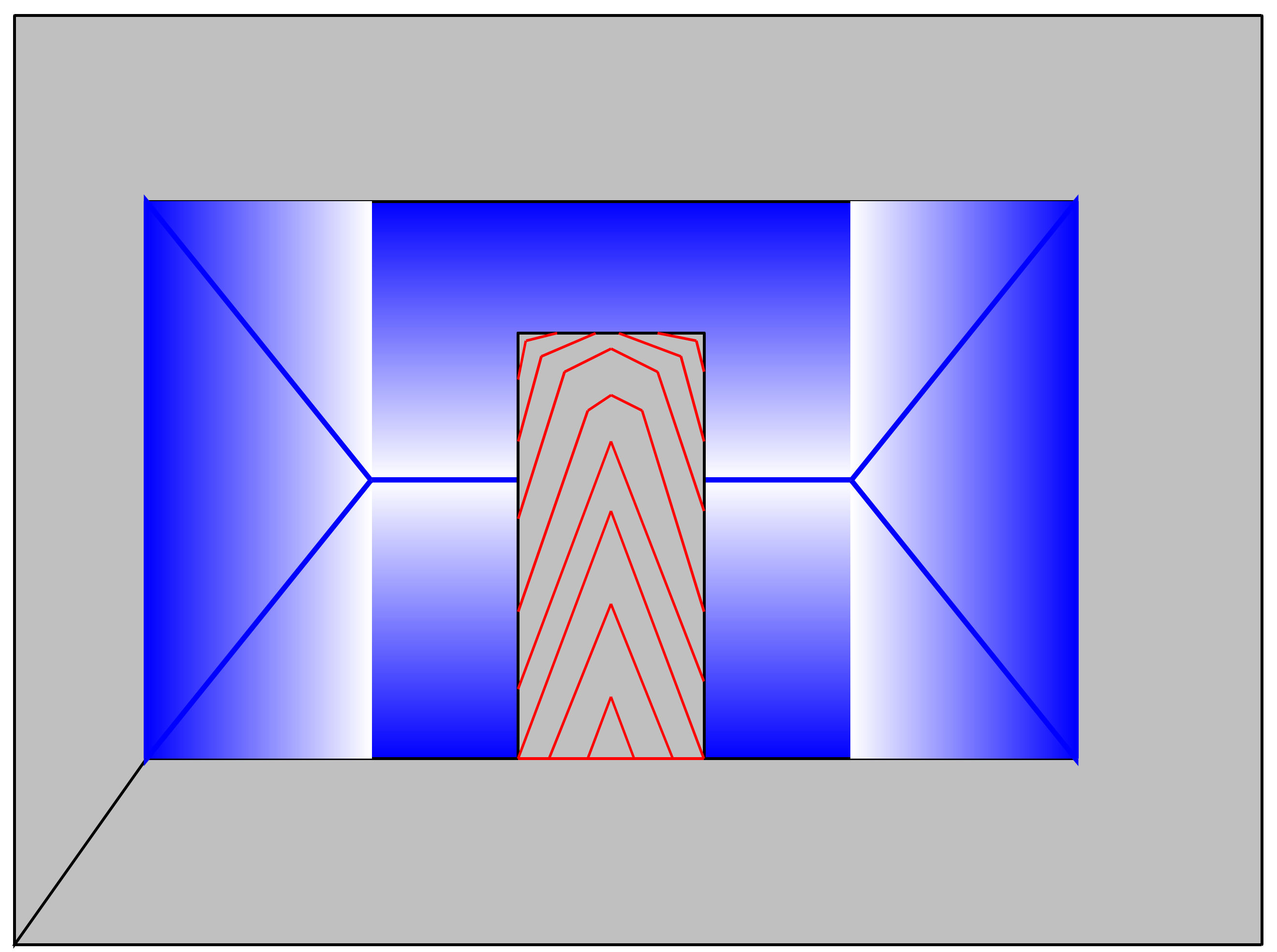


Etch Profile

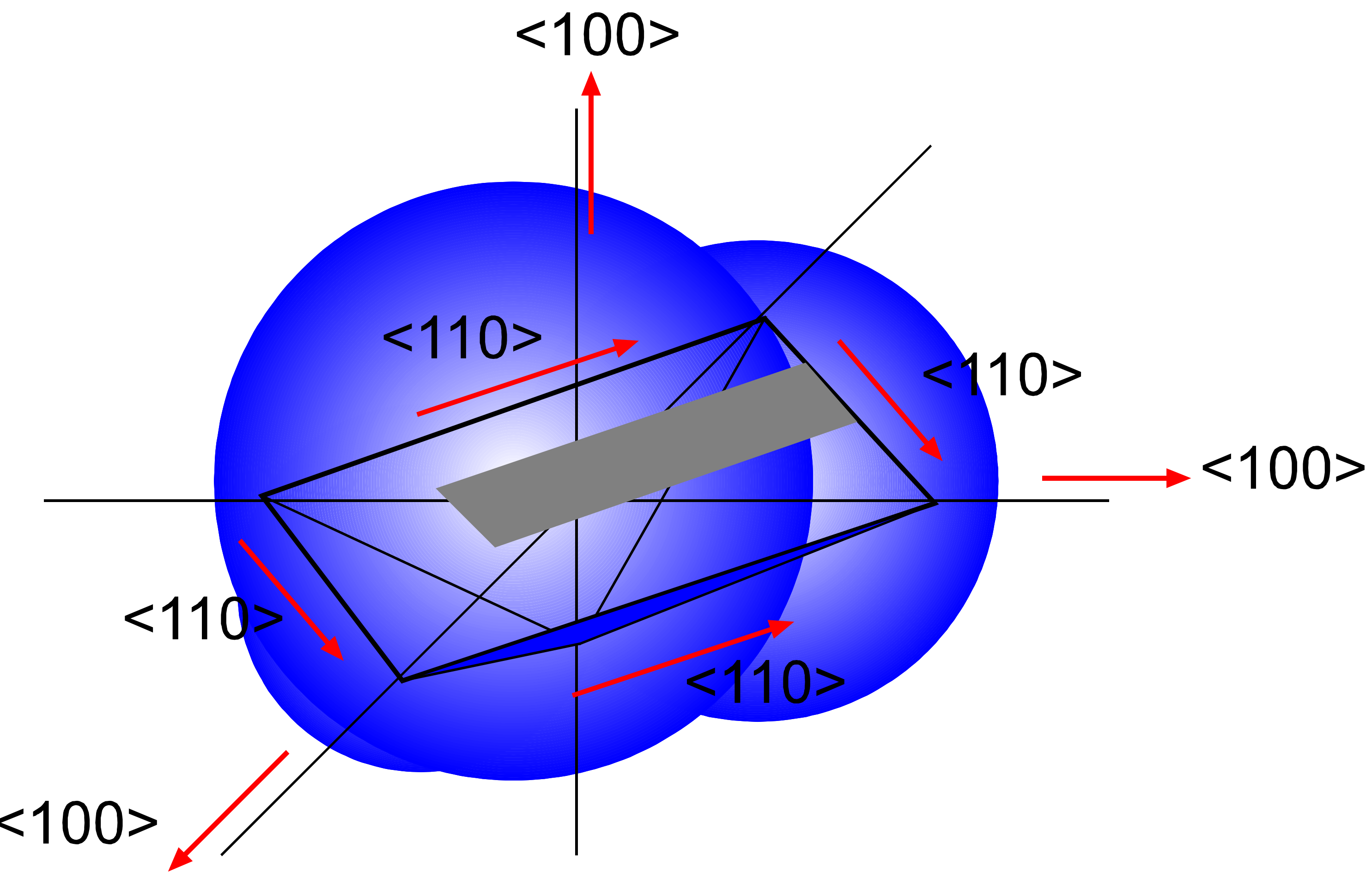
- Extended etching produces inverted pyramid by undercutting a convex structure (e.g. cantilever diving board beam in this case).
  - Red lines illustration etching profile evolution with time under the convex structure. (* p. 34, 35)



Etch Profile

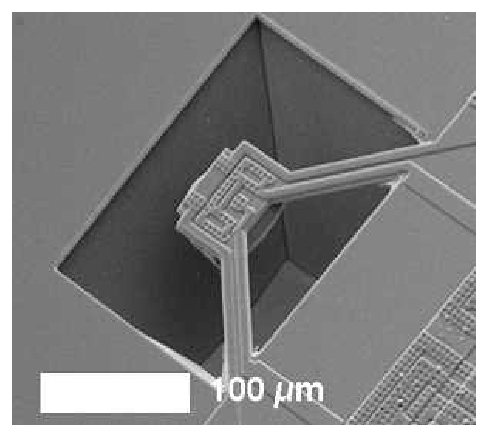


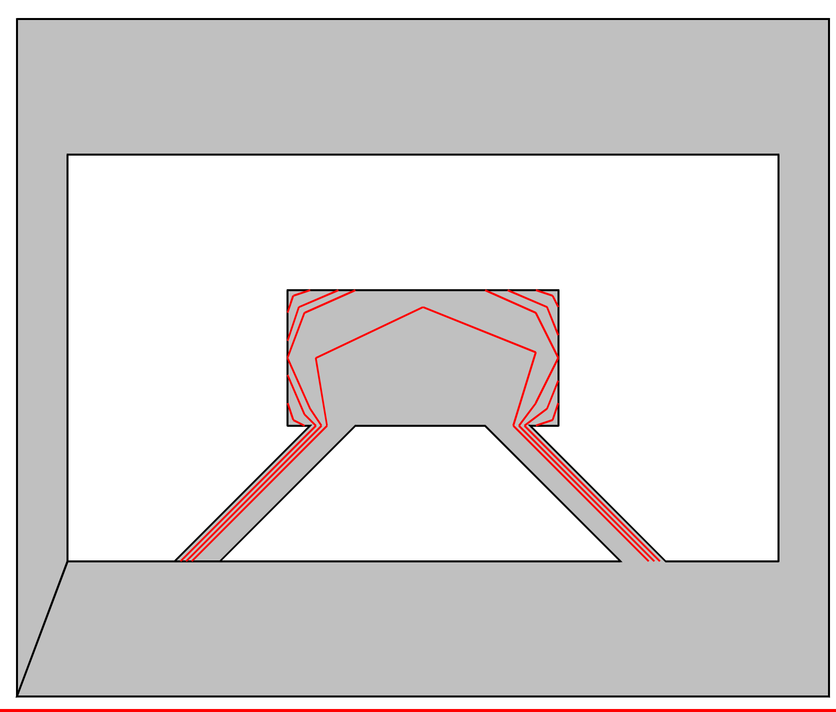
Perspective View of Etching Profile

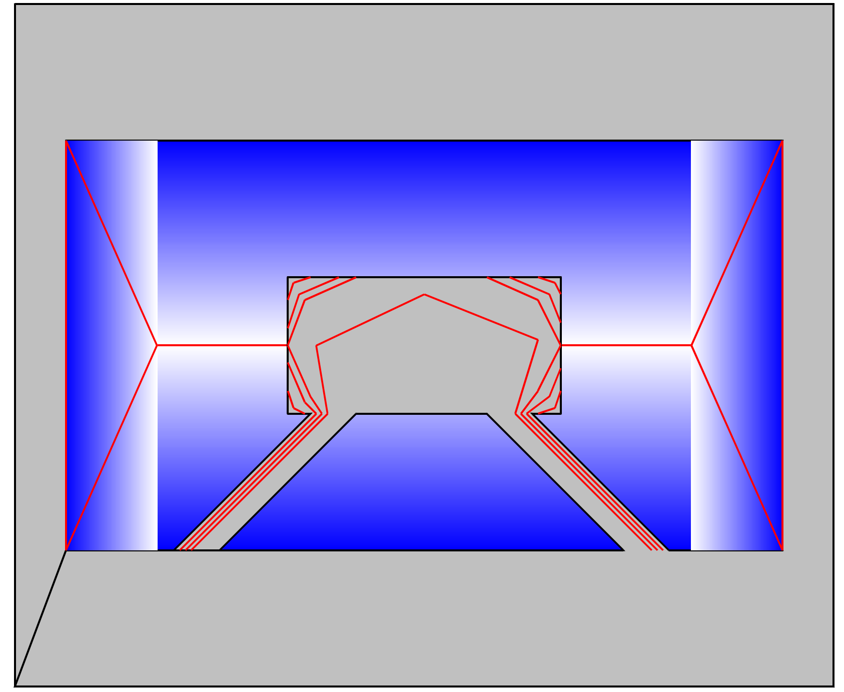


Real-life Case

- Convex corners are removed at fast etch rates.
  – See mask and simulation below.



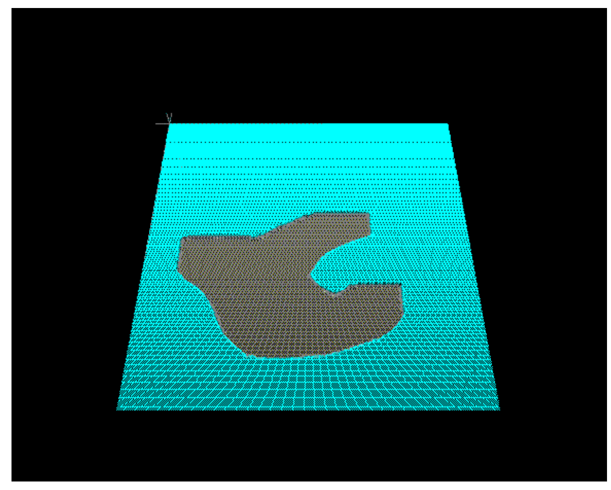


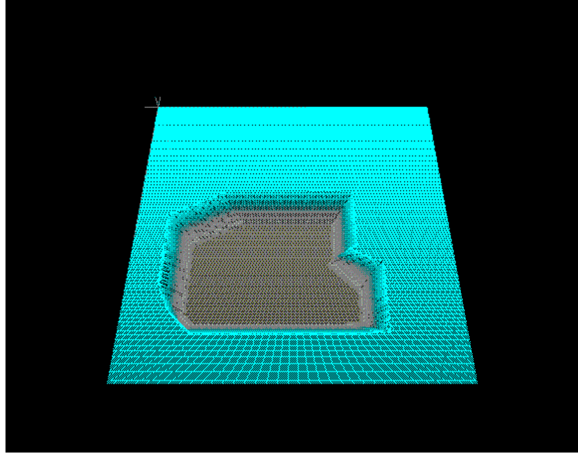


More Complex Cases

- Inverted pyramid is the final stable shape.
  - For an arbitrary shaped mask with transparent opening, the pyramidal shape is bound by the outside boundary.

mask





Etching Simulation Software

- As the mask shape becomes complex, it becomes more and more difficult to precisely predict the etching process and visualizing the results.
- Anisotropic Crystalline Etching Simulation (ACES) Software to the help.
- Demo copy of software can be found at http://galaxy.ccsm.uiuc.edu/aces

How does etchants remove silicon

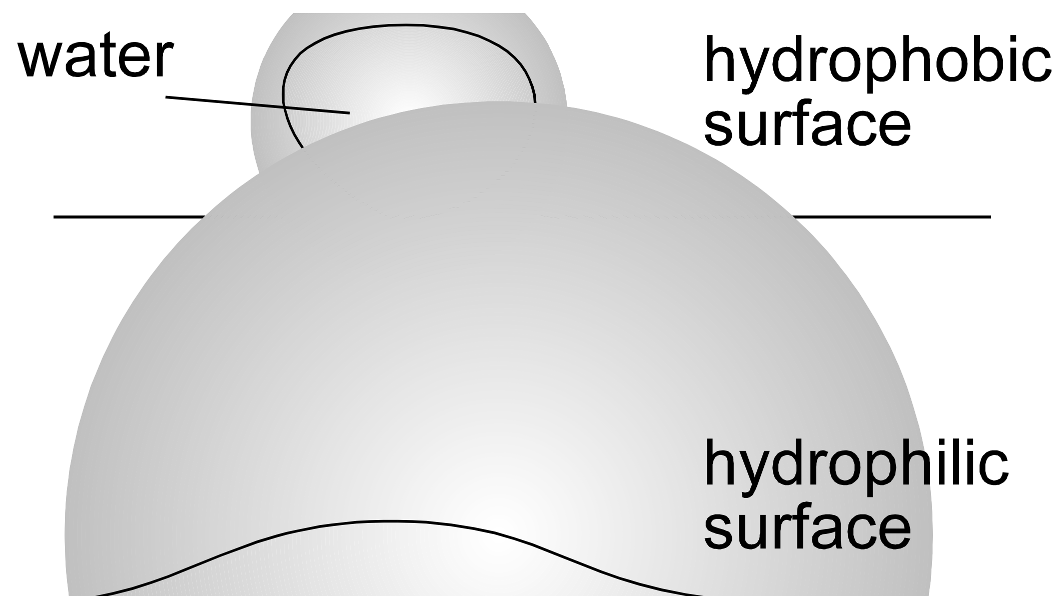
- According to commonly accepted theory, the silicon etchants contain oxidation and reducing agents.
  - The oxidation agents first turns silicon into silicon oxide
  - the reducing agents then etches the oxide away.

“Who Etches Who” - A Key to Designing Any Micromachining Process

- A comprehensive etch rate table can be found in the following resources:
  - paper titled “etch rates for micromachining processing” by K. Williams, JMEMS, Vol. 5, No. 4, p. 256, 1996.
  - Paper titled “silicon as a mechanical material” by Kurt Petersen, Bind Notes, Chapter 1.
  - Etch rate table, p. 30, * Kovacs text book.
  - Other chemical and physical handbooks (e.g. CRC handbook).
- A comprehensive understanding of etch rate is built through experience and research in the MEMS field.

Native Oxide (* Chapter 2, 4.2)

- Oxide formed on silicon when a bare and clean silicon is exposed to atmosphere at room temperature
  - typically tens of angstrom of oxide can be formed.
- How to determine whether native oxide has formed?
  - Pure silicon surface is hydrophobic
    - water will bead off.
  - Oxide silicon surface becomes hydrophilic.
    - Water will attach and spread.



Forming a Silicon Diaphragm (I)

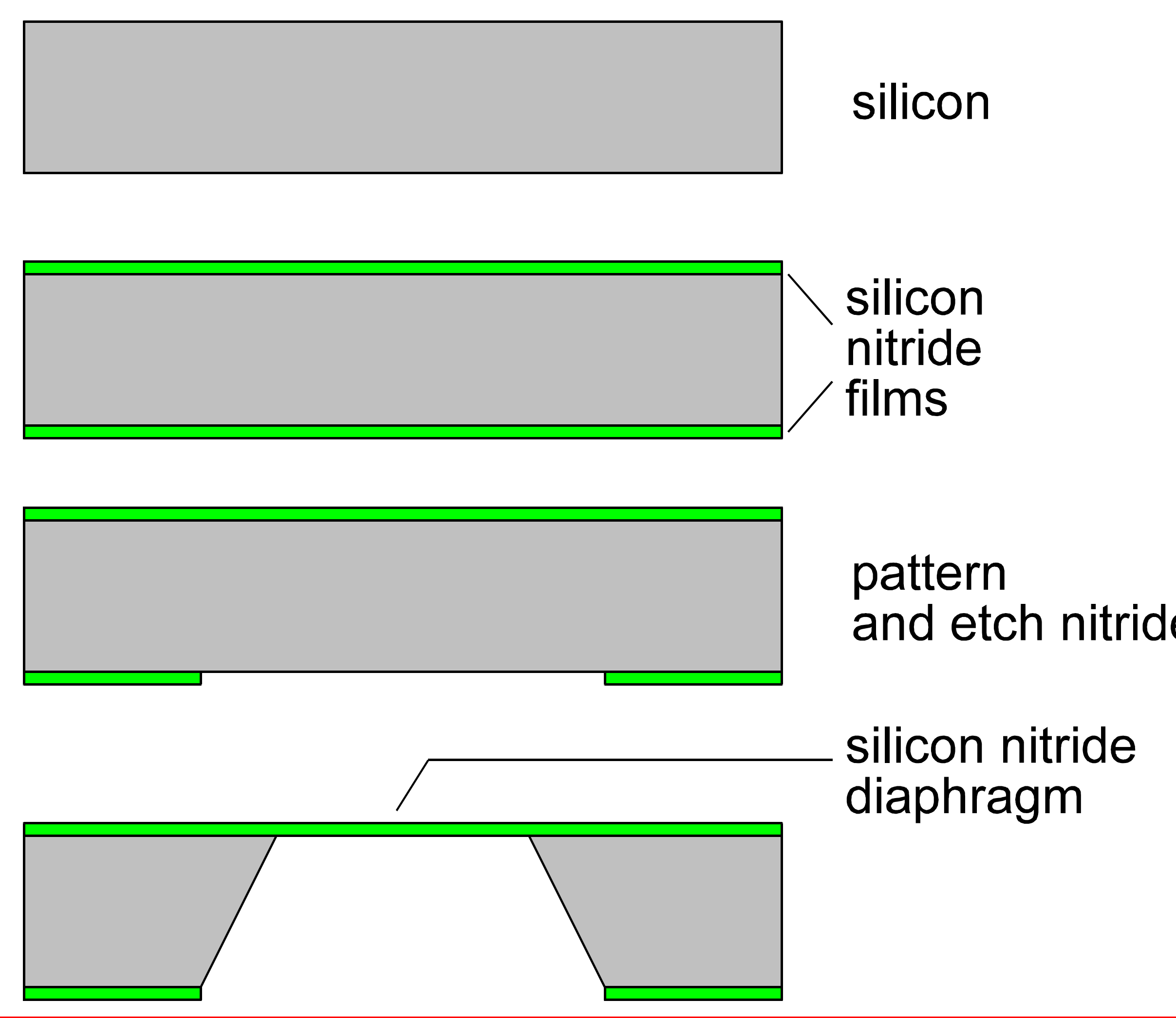
If the diaphragm is made of silicon nitride; because the etch rate of EDP and KOH on nitride is negligible, it is possible to etch the silicon by directly immersing nitride-coated wafers in etchant.

Nitride has tensile intrinsic stress.

Thickness typically < 1.5 μm.

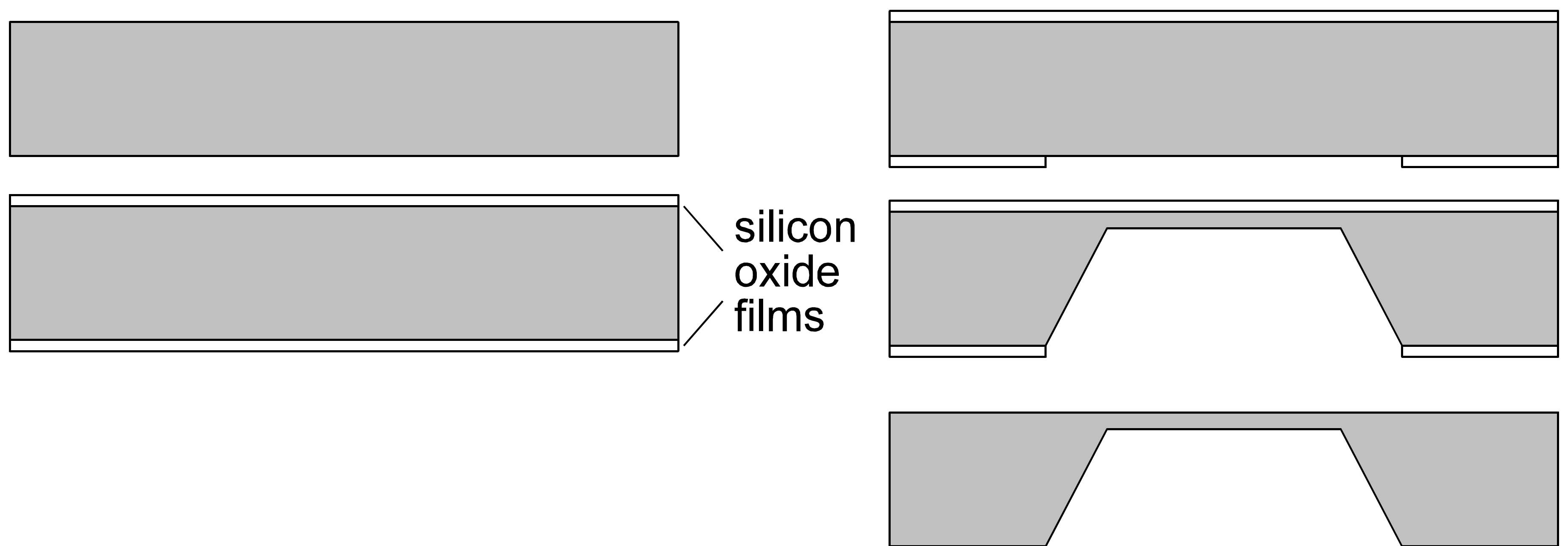
Not good for large thickness because the time to grow LPCVD nitride will be excessively long.

EDP or KOH etching are both possible.



Forming a Silicon Diaphragm (I)

- To form a silicon membrane (e.g. thickness > 3-10 μm), timed etch is to be used.
  - Use silicon oxide as the etching mask
    - oxide can be removed easily using HF after the device is made.
  - Use EDP or KOH to etch the materials
    - if KOH is used, attention must be paid to the thickness of oxide.
  - Calibrate the etch rate and the thickness of the wafer carefully.



Shortcomings of Timed Etch

- Etch rate varies with the age of the solution for Edp
- Etch rate is not uniform across the entire wafer area
  - some regions may be under etched while others over etched.
- Etch rate can also vary as a function of temperature and concentration.

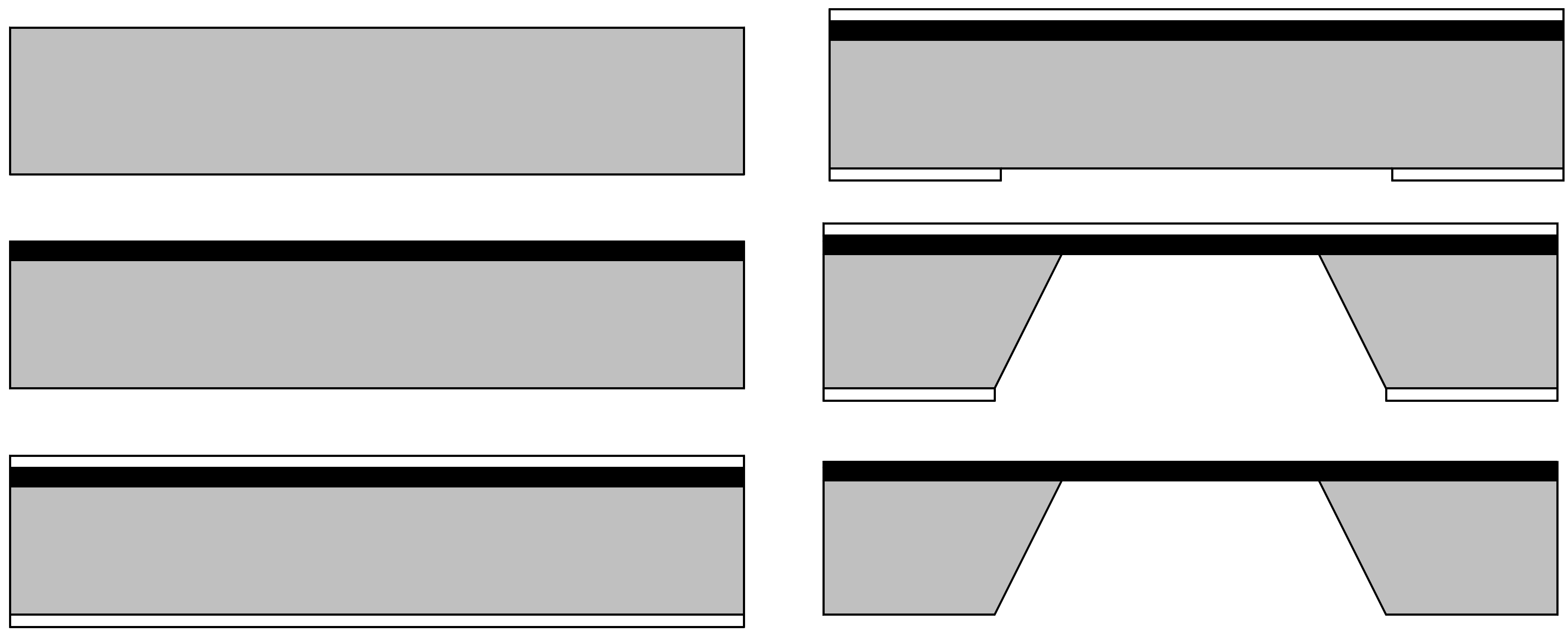
- Bottom line: timed etching must be used carefully and discriminatively in order to achieve efficiency in fabrication.

Etch Rate is a Function of the Doping Concentration

- Highly doped silicon exhibit much reduced etch rate compared with lowly doped silicon.
  - in EDP, doping concentration greater than 7×10^{19} cm^{-3} results in etch rate reduction of about 50;
  - in KOH, doping greater than 10^{20} cm^{-3} decreases etch rate by 20.
- Doping concentration can be specified by
  - diffusion doping
  - ion implantation + annealing (drive in)
  - wafer bonding

Forming Micro Diaphragm using Etch Stop Layer (* 46-47)

- Dope silicon with boron or phorphous to reach desired high doping concentration.
  - Doping is associated with much better uniformity and repeatability.
- Use oxide as a mask for back-side etching
- etching automatically stops when the doped layer is reached.

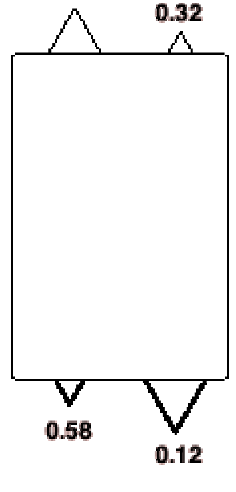


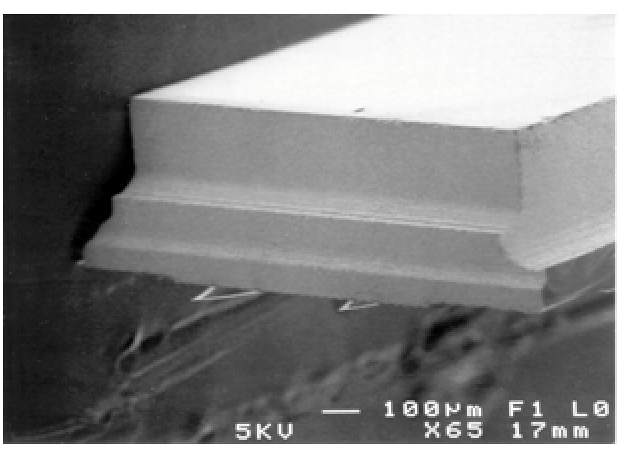
Examples of Applications

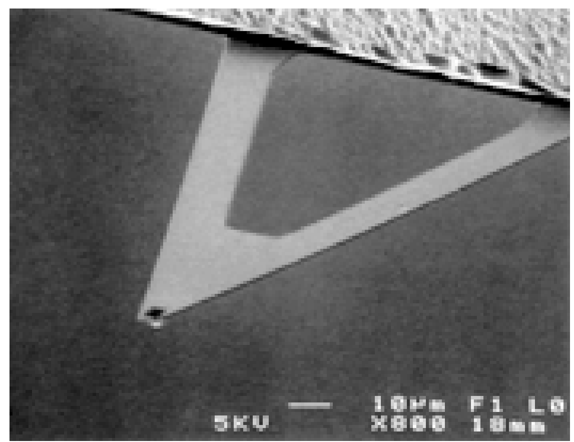
- Scanning probe microscopes
- Neuron probes
- micromachined RF devices

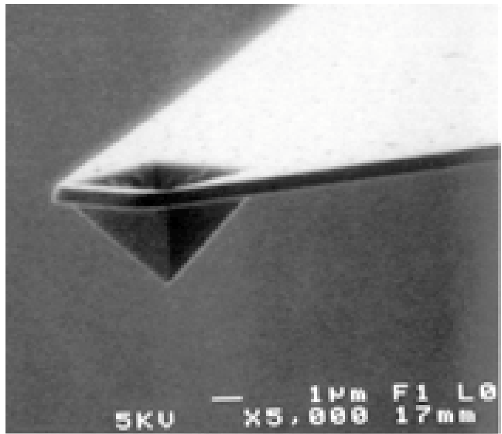
Digital Instruments SPM Probe Based on Stanford Process

- Www.di.com.
- Force (or Spring) Constants 0.58, 0.32, 0.12, 0.06 N/m*
- Nominal Tip Radius of Curvature 20 - 60nm
- Cantilever Lengths 100 & 200µm
- Cantilever Configuration V-shaped Reflective
- Coating Gold
- Shape of Tip Square Pyramidal









Stanford SPM

- Silicon nitride serving as the cantilever beam material.
- Step 1: oxidation of silicon with front surface being {100}.
- Step 2: pattern oxidation surface to create an open square with edges aligned to <110>.
- Step 3: etching of silicon in EDP or KOH solutions (KOH is possible is depth is not big.)
- The width of the opening and the depth is related.

$$t = \tan(54.75^o) \times \frac{w}{2}$$

silicon

silicon oxide

w

t

Stanford SPM (Continued)

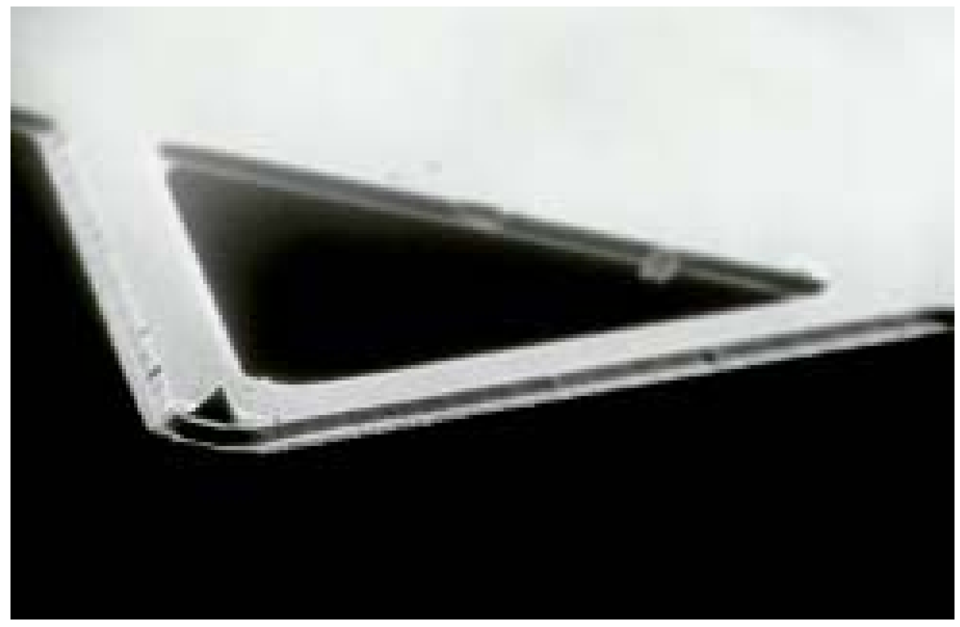
- Step 4: removal of oxide in HF, and deposit silicon nitride film (on both sides).
- Step 5: Pattern front side nitride and remove backside nitride using plasma etching.
- Step 6: bond a glass chip to the front side to serve as a handle.
- Step 7: Remove the entire bulk region to form the AFM/STM probe.

Relative Shortcomings of Stanford SPM

- Tip radius relatively limited due to etching shape (inverted pyramid)
  - as the tip is formed by “molded” silicon nitride, the shape is determined by the inverted pyramid.
- The silicon nitride stress is not repeatable and could result in non-uniform performance.

All Silicon SPM Probe

- Probe made of single-crystal silicon and thus has zero intrinsic stress.
- The tip is made of silicon such that it could be sharpened after the process is completed.



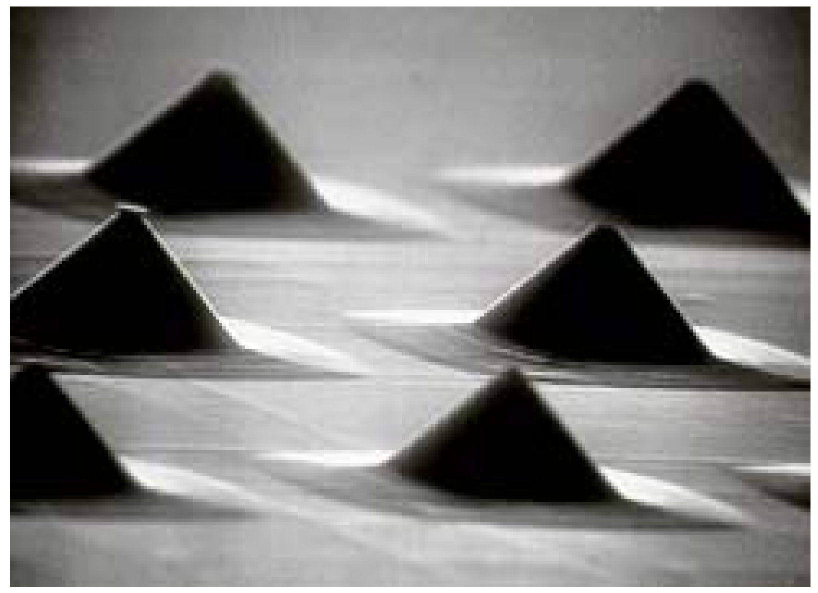
All Silicon SPM Probe Process

- *Monolithic fabrication process for an SPM probe. (a) structural layers on a starting 4-in wafer; (b) silicon oxide mask is patterned on the front side of the wafer; (c) anisotropic etching produces a pyramid-shaped tip; (d) cantilever beams are formed using reactive ion etching; (e) back-side etching releases the cantilever beam.*
- *Starting wafer: epitaxy silicon + buried highly doped silicon + regularly doped silicon substrate.*

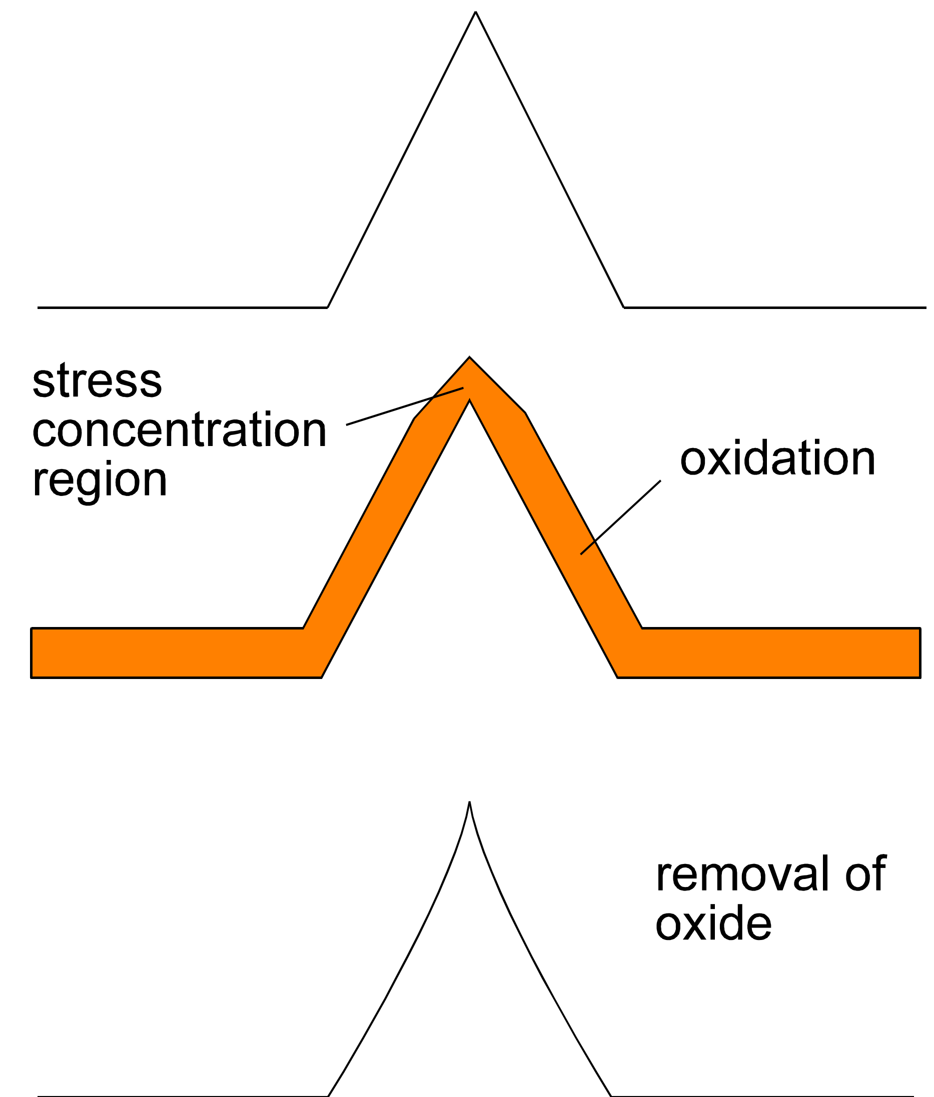
epitaxial layer
doped layer
bulk silicon
(a)
oxide mask
(b)
tip
(c)
beam
(d)
(e)

Tips can be sharpened

- Oxidation sharpening: low level oxidation in regions with compressive stress.

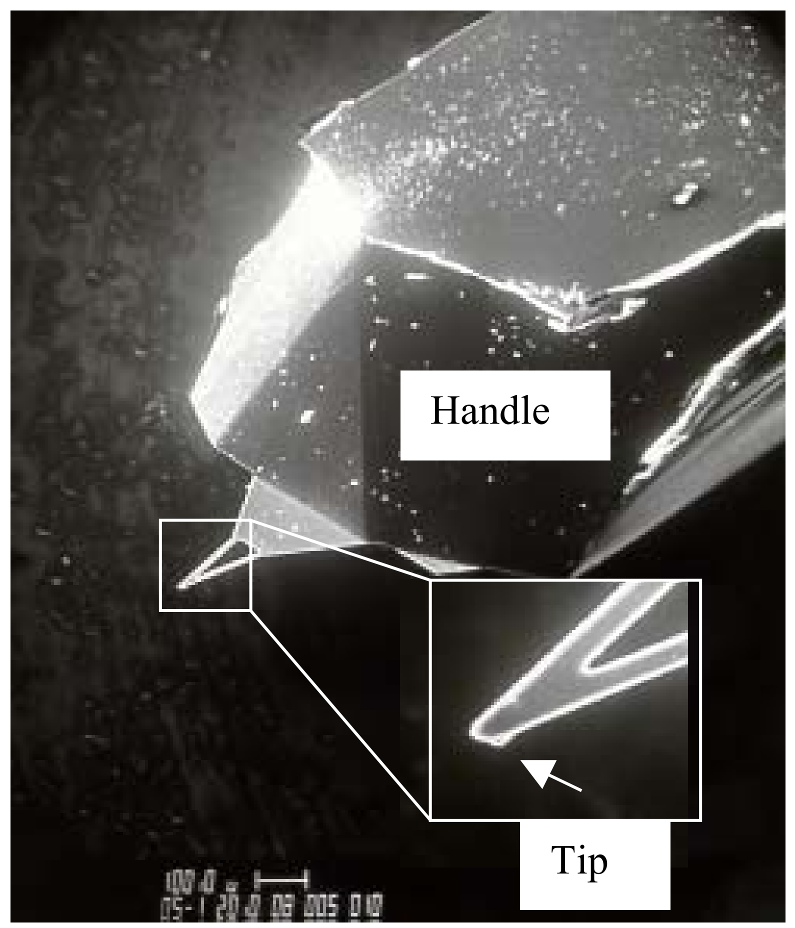


Oxidation Sharpening Mechanism



All Silicon SPM Probe

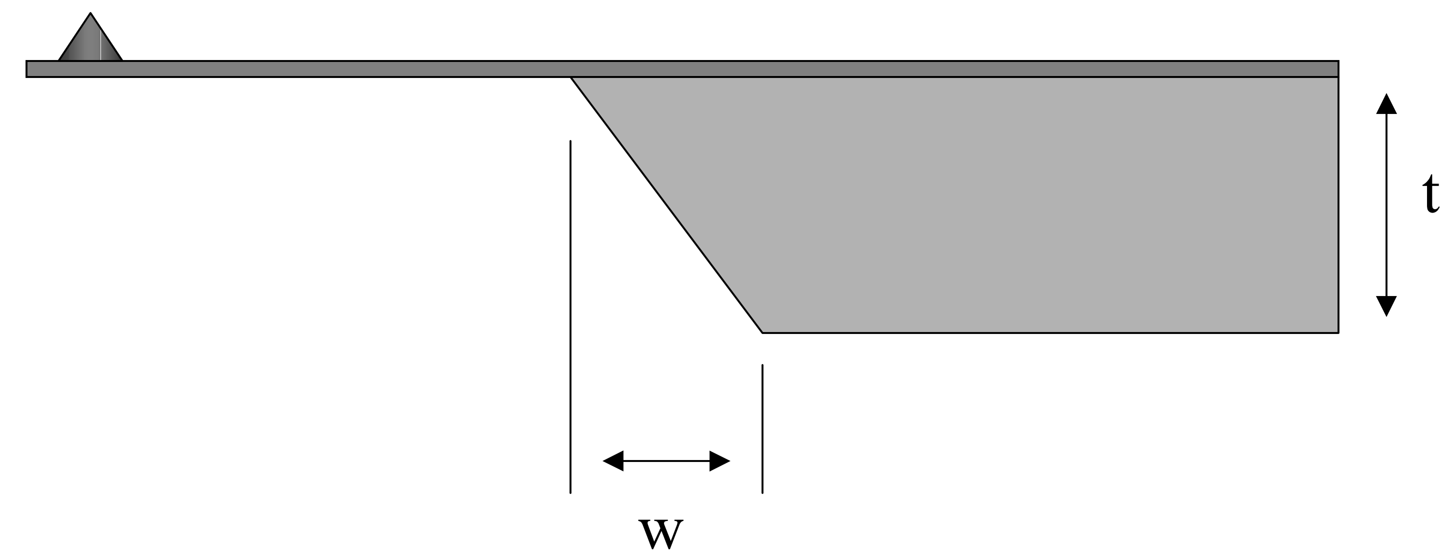
- Advantages
  - zero stress beam structural material.
  - Tip can be further sharpened using oxidation process.



Calculate the Beam Length.

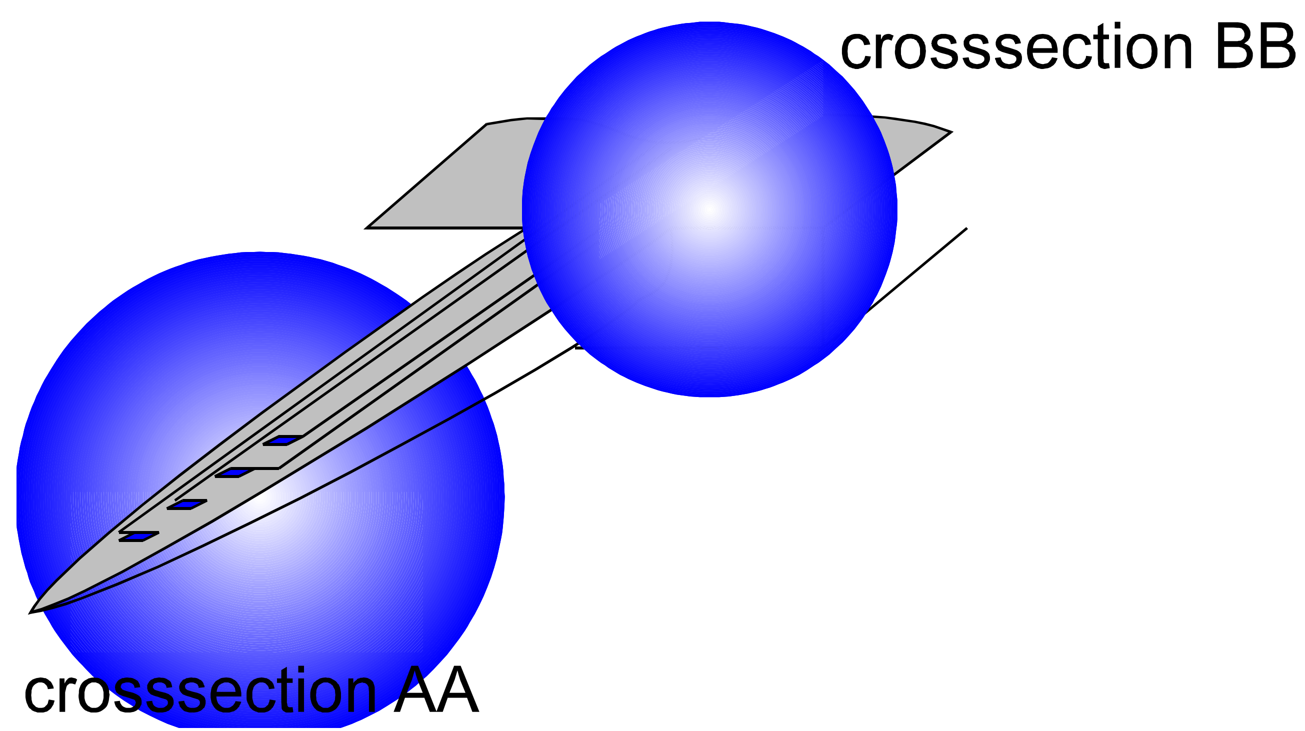
- The length is the beam is different from what is defined on the backside of the wafer. The difference is w. The relationship between w and the thickness of the wafer is

$$t = w \times \tan(54.7^0)$$



Neuron probes (U. Michigan)

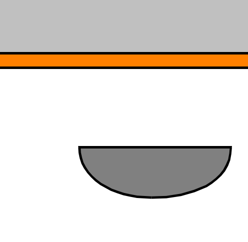
- Single crystal silicon neuron probe.
- Shank is formed by heavily doped regions.

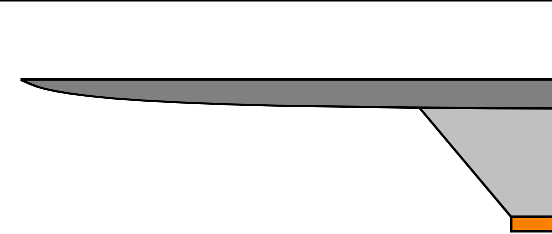


AA BB

Neuron probe

- Step 1: starting with low doped silicon.
- Step 2: protect both front and backside with oxide (thermal oxide)
- Step 3: open regions on front side where silicon is exposed.
- Step 4: thru the exposure windows, dope underlying silicon. Regions covered by oxide will not be doped.
- Step 5: Remove bulk silicon selectively to produce the free-standing beams.





<111> Wafer

Surface-Bulk Micromachining (SBM)