Simulation exercises using SCHRED

(The code is accessible on line: www.nanohub.purdue.edu)

1. Using SCHRED, plot the conduction band profile, electron density and total charge density in a MOS capacitor with N_A=5×10^{17} cm^{-3} and d_{ox}=3 nm. For the applied voltage, use V_G = 0.5 V and V_G=1.0 V. Assume classical charge distribution, Maxwell-Boltzmann statistics and metal gates. For the parameter dksi in the SCHRED input file use dksi=0. The temperature equals T=300 K. From the graph or the numerical data estimate the magnitude of the surface potential and use this result to calculate the depth of the depletion regions. How do the values calculated for the two gate voltages compare to what the plots for the conduction band profile or the total charge density give. For the semiconductor dielectric constant use $k_s\varepsilon_0 = 1.05\times10^{-10}\,F/m$.

2. Simulate an MOS capacitor structure with the following parameters: oxide thickness t_{OX} = 1.5 nm, substrate doping N_A = 10^{19} cm^{-3}, metal or polysilicon gates. Perform the following simulation runs:

   - Metal gates, semi-classical charge description, Maxwell-Boltzmann statistics.
   - Metal gates, semi-classical charge description, Fermi-Dirac statistics.
   - Metal gates, quantum-mechanical charge description (e_nsub1=4, e_nsub2=2)
   - Poly-silicon gates with N_D=2×10^{19} cm^{-3}, quantum-mechanical charge description
   - Poly-silicon gates with N_D=6×10^{19} cm^{-3}, quantum-mechanical charge description.

   Answer the following questions:

   - What is the magnitude of the capacitance degradation and the effective oxide thickness modification for each of these models for gate biases of 2 V and 2.5 V.
   - What is the corresponding threshold voltage shift?
   - Justify your results using physical reasoning.